Advantage of Floating Gate B4-Flash over Retention Reliability after Cycling - Characterization by Variation of Transconductance -

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Abstract **– This paper describes the reliability characteristics evaluation results of floating gate type B4-Flash (Back Bias assisted Band-to-Band tunneling induced Hot Electron injection Flash) with statistics. Data retention reliability of B4-Flash with N+gate and P-channel memory cell utilizing B4-HE program and FN channel erase is evaluated extensively under bake temperature of -24C to 250C up to 7000hrs after 1k to 1M E/W cycles, by novel evaluation method of correlating Vt shifts and gm variations. No leaky bit failure can be seen in B4-Flash with thicker than 9nm tunnel oxide and the Vt shifts during retention bake is associated with electron detrapping and move into floating gate from tunnel oxide, which is verified by correlating Vt shifts and gm variations. Tunnel oxide thickness dependence on retention reliability is also studied and confirmed to have excellent retention characteristics under 150C after 100k cycling. In the case of 7nm tunnel oxide thickness device, some leaky bits due to stress induced leakage current (SILC) can be seen even in B4-Flash, nevertheless number of tail bits is remarkably reduced compared with that of conventional N+gate, N-channel NOR flash. According to all the obtained results show that B4-Flash can achieve excellent retention reliability after cycling with high speed programmability.**

Introduction

Stress induced leakage current is a well-known and serious phenomenon which deteriorates flash memory reliability and restricts its scaling. SILC related leaky bits can be seen in flash memories with N-channel cells after E/W cycles[1]. Reliability characteristics would be influenced erase write mechanisms and memory cell transistor polarities. According to the memory cell transistor polarity effects, P-channel flash memories utilizing CHE or FN programming is reported to have superior reliability compared to N-channel flash memories[2] and other characteristics[3]-[5]. In terms of combinations of programming mechanisms and memory cell transistor polarities, band-to-band induced hot-electron (BBHE) injection programming in N+gate P-channel cell less degrades tunnel oxide quality than that of the CHE and Fowler-Nordheim (FN) tunneling in N+gate N-channel cell[6]. However, opposed experimental result on this issue has also been reported[7]. It seems that a further investigation with statistics is necessary regarding P-channel cell with BBHE injection scheme for programming.

In this paper, we investigate retention characteristics of the cycled B4-Flash memory[8]-[10] with statistics. A technique to pursue variation of intrinsic gm of the memory cell has been employed. Vt shifts during retention is discussed from the view point of correlation with gm variation.

Experimental

Evaluated P-channel floating gate flash memory devices having tunnel oxide thickness of 10.8, 9 and 7nm have been fabricated using a conventional 130nm N-channel NOR flash memory process. The cells are programmed by B4-HE injection and erased by uniform channel FN tunneling. E/W cycling was performed from 1k to 1M count. Data retention evaluations were carried out from -24C to 250C up to 7000hrs. 64kb regions out of a 512kb block have been evaluated by using 4Mb test chips[9].

The gm was derived by comparing Vt distributions measured at two sensing current, as shown in Fig.1. Variation of gm as a function of E/W cycles is shown in Fig.2. It should be noted that the gm improves by cycling, and shows a peak at around 1k cycling. This may be because that a part of the trapped electrons plays a substantial role to decrease scattering centers or surface-state densities for holes in channel region[11]. Thus, gm gives a good indication of the quantity of trapped charge in the tunnel oxide. These results suggest that the excess electron trapping occurs near the drain end where B4-HE injection is carried out.

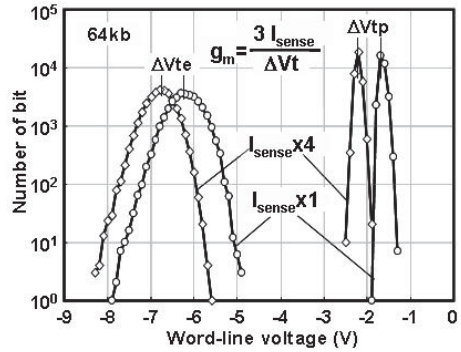

Fig.1 Method of gm derivation by comparison of two Vt distributions at different sensing current.

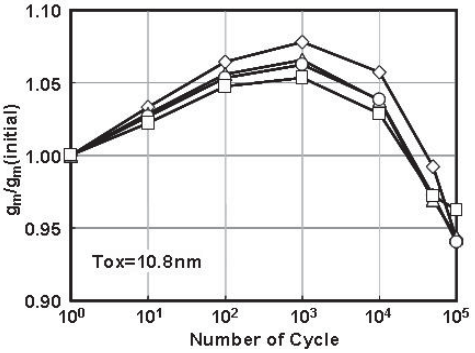

Fig.2 P-channel B4-Flash gm variations as a function of E/W cycling count for several chips.

Results and Discussion

Typical Retention Characteristics of B4-Flash

Typical long-term retention characteristics of the B4-Flash have been evaluated using 10.8nm oxide cells. Retention characteristics at 250C for 7000hrs after 10k cycled cells are shown in Fig.3. Rather large Vt shift can be seen in erase state, while Vt shift in program state is quite small. In either case, no excursion bits can be seen and retention characteristics shown in Fig. 3 is quite satisfying which has never obtained in conventional flash. Fig.4 shows the erase state typical bit retention Vt shift characteristics dependencies on bake temperature, in which the activation energy is extracted as 1.7eV. Monotonic temperature dependence on Vt shift can be seen in Fig. 4. SILC related leakage said to have its peak around 50C to 100C[12], which means that there's no SILC related retention Vt shift in B4-Flash. In order to clarify the origin of these excellent retention properties of B4-Flash memory, dependencies on cycle count, storage

temperature and tunnel oxide thickness have been extensively investigated and compared to that of conventional N-channel flash.

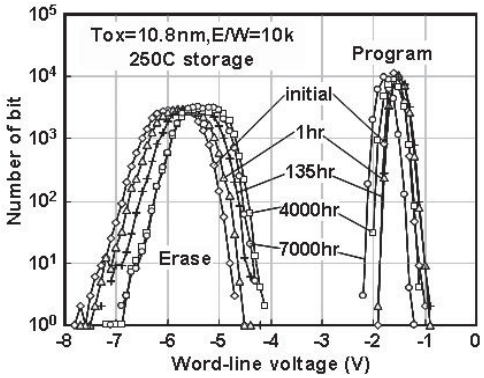

Fig.3 Variation of Vt distributions at 250C storage after 10k cycling.

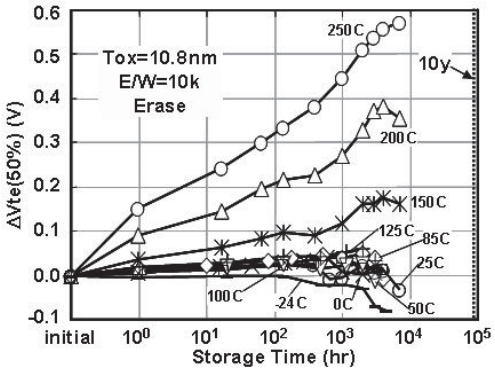

Fig.4 Temperature dependencies of the typical-bit Retention characteristics in erase state for 7000hrs after 10k cycling.

Cycle Count Dependence

150C retention characteristics for 3000hrs after 1M cycled cells with 10.8nm oxide are shown in Fig.5. We don't see any defective bits in both program and erase states and both of Vt distributions move to positive direction. These results suggest that increase of amount of negative charge in the floating gate or hole detrapping from the tunnel oxide to substrate must have occurred for both states. Cycle count dependencies of the worst-bit retention characteristics of 10.8nm oxide cells are shown in Fig.6. Retention Vt shifts increase in accordance with cycle count in erase state, however, Vt shift in program state is less than 0.2V for all cycle count. Furthermore, the worst-bits do not show an anomalous behavior in all cycle count, which indicates that SILC leaky tail-bit does not appear even after 1M cycling.

Temperature Dependence

Fig.7 shows the temperature dependencies of the worst-bit retention characteristics of 10.8nm oxide cells. This indicates that the worst-bits do not show an anomalous behavior in all storage temperature, which means again that we don't see any SILC related retention Vt shifts in B4-Flash. Temperature dependencies of the typical-bit retention characteristics in erase state after 100k cycling are shown in Fig.8. Activation energy is extracted as 1.2eV, which is smaller than that of 10k cycling case and is the same value as the activation energy of electron detrapping in cycled N-channel cells[13]. Corresponding variations of gm are shown in Fig.9. The gm degrades during retention storage for all storage temperatures.

Figs.10(a) and (b) show the correlations between Vt shift and gm variation in case of different temperature storage and different cycle count storage, respectively. Coordinates of each point in Fig.10

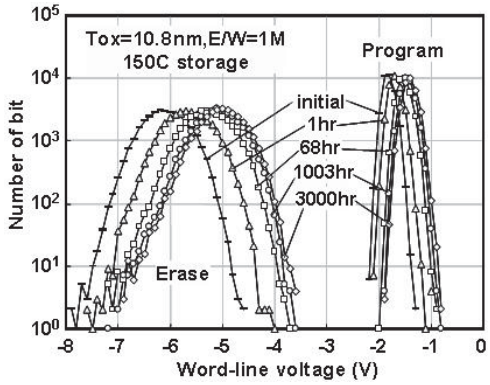

Fig.5 Variation of Vt distributions at 150C storage after 1M cycling with 10.8nm oxide cells.

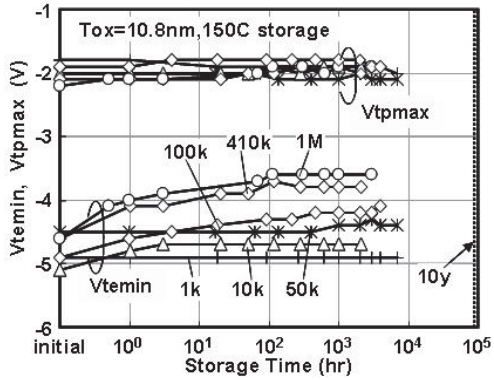

Fig.6 Cycle count dependencies of the worst-bit retention characteristics for 3000hrs at 150C storage.

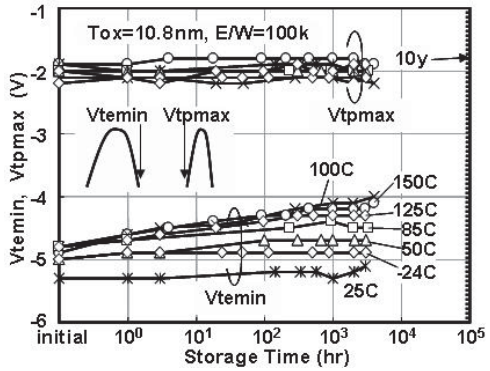

Fig.7 Temperature dependencies of the worst-bit retention characteristics for 4000hrs after 100k cycling.

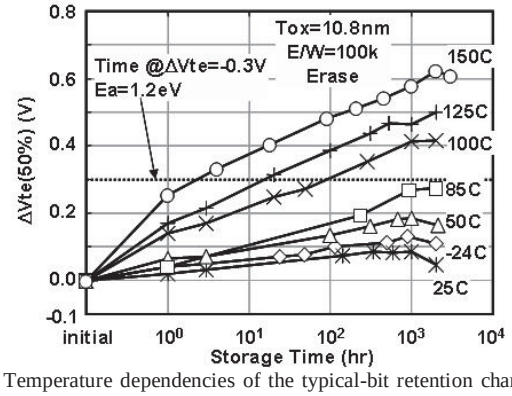

Fig.8 Temperature dependencies of the typical-bit retention characteristics in erase state after 100k cycling.

are derived from corresponding point in Figs. 8 and 9. It can be seen that the measured results of all the storage temperatures and all cycle counts show the same proportionality relation, which means that Vt shifts and gm variation are strongly correlated to each other.

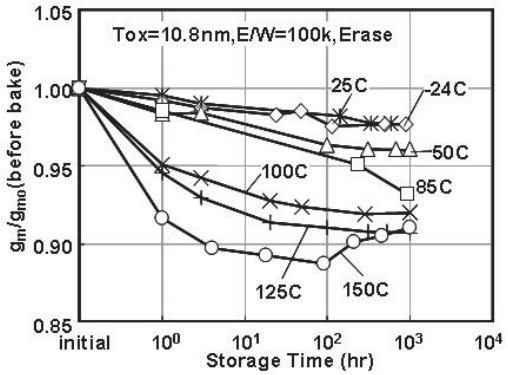

Fig.9 Temperature dependencies of variation of gm in erase state after 100k cycling.

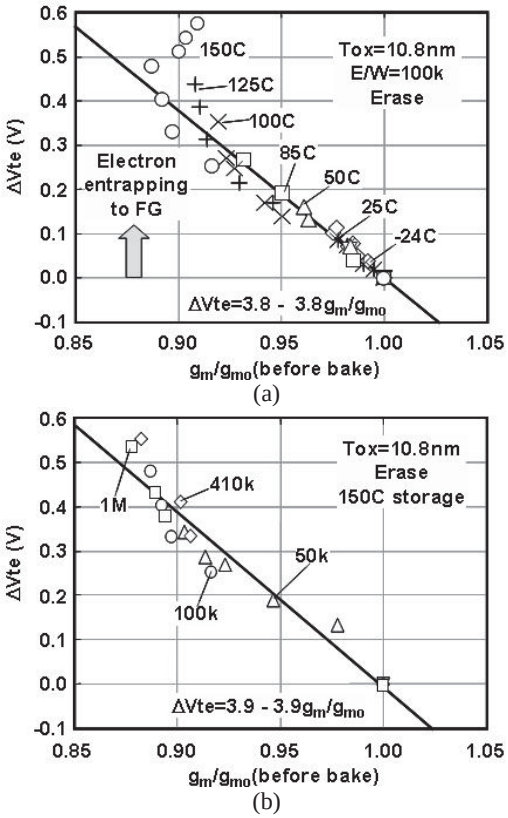

Fig.10. Correlation between Vt shift and gm variation during storage in erase state, temperature(a) and cycle count dependence(b).

Consideration on Charge Detrapping Model

Electrons locally trapped in the oxide enhance the electric field near the interface[11]. As a consequence, near the drain end, effective channel length is modulated to be shortened by the electric field[14], resulting in gm increase and Vt decrease. Therefore, the degradations of gm shown in Fig.10 suggest the occurrence of electron detrapping. From the fact that Vt in erase state moves to positive direction as shown in Figs.5 and 8, the electrons should be detrapped to the floating gate. From the experimental results shown in Fig.10, Vt shift can be expressed by $\Delta Vte=4(1 - g_m/g_{mo}) = -4\Delta g_m/g_{mo}$, $\Delta g_m = g_m - g_{mo}$. Assuming that the trapped electrons play a role to decrease the effective channel length, $\Delta g_m/g_{mo} = -\Delta L_{eff}/L_{eff}$. In Fig.10, it can be considered that 0.4V shift of Vte corresponds 10% change of the effective channel length.

In the program state after 1M cycling, Vt distributions move to positive direction and shift itself is smaller than that of erase state as shown in Fig.5. This result suggests that SILC does not appear but electron detrapping from tunnel oxide to floating gate occurs in the program state even after 1M cycling. The electron detrapping to floating gate would be suppressed compared with that of erase state due to less electric field during retention bake than that of erase state.

The gm variation tends to stop over 100hrs at 150C as shown in Fig.9, while Vt shift occurs continuously as shown in Fig.8. This discrepancy between Vt shift and gm variation suggests that electron detrapping occurs at the position where trapped charge does not contribute gm modulation.

Tunnel oxide thickness Dependence

Retention Vt shifts of 100k cycled cells with different tunnel oxide thickness of 10.8, 9 and 7nm at storage temperature of 150C for 2000hrs have been evaluated, as shown in Figs. 11(a), (b) and (c), respectively. It was reported that a remarkable electron loss as tail-bits due to SILC is found in the CHE-programmed and FN-erased N-channel NOR cells having 8.5nm oxide[15]. However, excellent retention characteristics were confirmed in the B4-Flash cells with 9nm oxide or thicker.

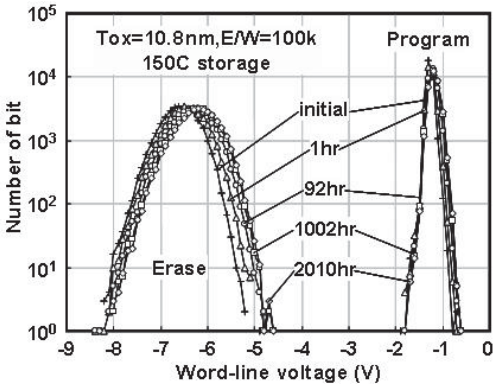

Fig.11(a) Variation of Vt distributions at 150C storage after 100k cycling of 10.8nm oxide cells.

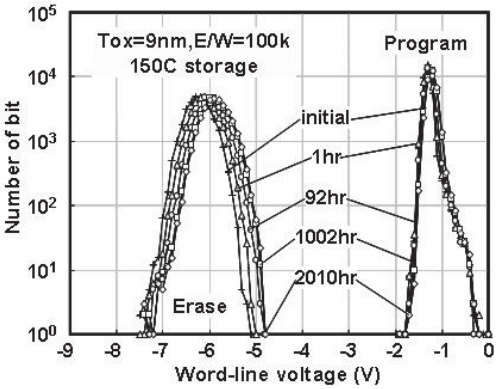

Fig.11(b) Variation of Vt distributions at 150C storage after 100k cycling of 9nm oxide cells.

In the case of 7nm tunnel oxide, no average Vt shift but leaky bits which are considered not to due to electron detrapping into floating gate but due to SILC, can be seen in the erase state (Fig. 11(c)). This is quite different retention characteristics from that of 9nm tunnel oxide and thicker. Comparison of SILC leaky bits statistics of 7nm oxide cells at 25C storage of an conventional N-channel NOR[15] and B4-Flash are shown in Fig.12. It can be seen that number of the leaky bits in 10k cycled B4-Flash is remarkably reduced compared to

that of the N-channel cells. We can conclude again that B4-Flash achieves higher retention reliability than that of conventional N-channel flash memories.

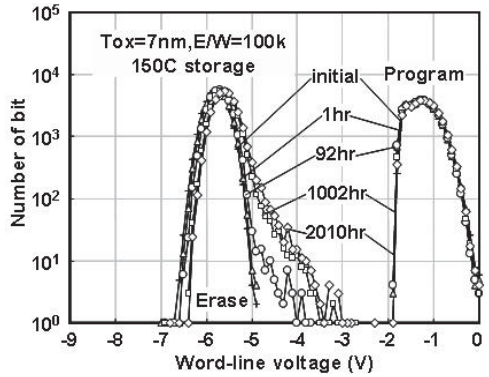

Fig.11(c) Variation of Vt distributions at 150C storage after 100k cycling of 7nm oxide cells.

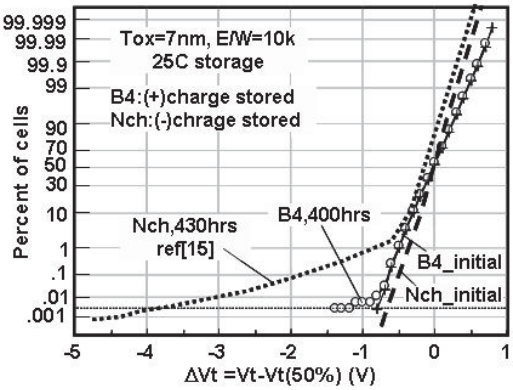

Fig.12 Comparison of SILC tail-bits of the 7nm oxide cells at 25C storage of an N-channel[15] and B4-Flash.

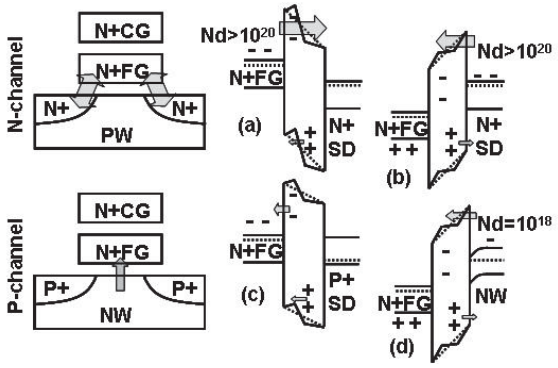

Fig.13 Band-diagram and the possible SILC spot comparisons of an N-channel and B4-Flash cells with N+ floating gate, band-diagram comparisons at gate edge of (-)charge stored state:(a)(c), and of (+)charge stored state at the most leaky position for both cells:(b)(d). (c) indicates an advantage of band configuration. (d) explains cathode doping level of B4-Flash.

Consideration of B4-Flash retention superiority over conventional flash

Fig.13 compares schematic band-diagram and the possible SILC spot of an N-channel and P-channel B4-Flash cells with N+ floating gate. In retention of the cycled N-channel cells, it was reported that 85% of the tail-bits have the SILC spot on the drain side[16]. For the P-channel cell with negative charged floating gate state, it is considered that the electric field at the gate edge decreases by Eg/Tox. This is because that flat-band difference between the diffusions and floating gate are reduced by 1.1V compared with N-channel cells, as compared in Fig.13 (a) and (c). Moreover, this band-configuration of B4-Flash also reduces both FN electron current and anode hot hole injection at the gate edge during the erase operation, so that the generation of SILC spot at gate edge is strongly suppressed compared with conventional N-channel NOR flash. On the other hand, the anode hot hole injection during FN electron tunneling is considered to be the main cause to degrade oxide integrity in conventional N-channel NOR and NAND flash cells.

In case of positively charged floating gate state, SILC spot of 7nm oxide B4-Flash is considered to be located in the channel region as shown in Fig.13. This is because that channel region would be stressed during FN erasure in B4-Flash, where tunnel oxide quality must be higher compared with gate edge region. Comparisons of SILC tail-bits distribution as shown in Fig.12 corresponds to the band-diagram comparison indicated in Fig.13 (a) and (d). For conventional N-channel NOR cells, band-diagrams of both program and erase state are symmetry as shown in Fig.13 (a) and (b), because both electrodes of the diffusion and floating gate are heavily doped N type, so that the electric field during retention is determined by the difference between the intrinsic Vt and program/erase Vt of the cells. It has been reported that lower phosphorus doping level in the floating gate of the N-channel cells decreases the SILC drastically[17]. Therefore, it is considered that this cathode doping level effect also contributes to improve SILC of the cycled B4-Flash cells due to channel region of B4-Flash act as quite low level doped cathode during erase state retention.

Conclusions

B4-Flash with N+gate and P-channel cell utilizing B4-HE program and FN channel erase has been confirmed to have excellent retention reliability of more than 10 year under 150C after 1M E/W cycles. We have evaluated B4-Flash retention characteristics by novel evaluation method of correlating Vt and gm variations. We found out that retention Vt shift of B4-Flash is caused by detrapping of electrons trapped in the tunnel oxide during cycling, and moving into floating gate. This retention Vt shift mechanism is not caused by DC leakage of SILC, so that Vt shift of B4-Flash retention must be saturated in certain level. Those superior reliability characteristics in B4-Flash can be explained by its band configurations.

According to these superiorities in reliability, B4-Flash can utilize thinner tunnel oxide such as 9nm thick, compared to conventional flash. Thus B4-Flash can achieve fast erase capability equivalent to NAND with high speed programmability of 100MB/sec[8-10]. These features boost B4-Flash to be the best suited flash memory for next generation code storage applications such as those for mobile phones and automotives with high reliability. Furthermore, thanks to its excellent scalability down to 50nm and below, future high speed and highly reliable SSD application can be realized by B4-Flash.

References

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