A 1.8V 4Mb Floating-Gate NOR Type B4-Flash Test Chip for 100MB/s Programming Speed

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Abstract

A 1.8V 4Mb floating-gate Flash test chip utilizing Back Bias assisted Band-to-Band tunneling induced Hot Electron (B4-HE) injection mechanism (B4-Flash) has been fabricated. Double Source Line Architecture (DSLA) and Selective Verifying Method (SVM), applied to NOR arrayed B4-Flash enables to achieve 100MB/s programming speed. The MLC capability of B4-Flash memory is also shown by realizing three levels of programmed Vth distribution with 0.8V width.

Introduction

Higher program speed of Flash memories is one of the most emergent requirements from the huge semiconductor NVM market. NAND Flash achieves high program speed of 10MB/s [1] among all Flash memories, which is 1/10 to that of HDD's, and conventional NOR Flash does much less. We proposed new program mechanism, B4-HE, and confirmed its high speed and highly efficient program properties, which showed the possibility to realize 100MB/s programmability [2]. In this paper, we implement B4-HE to floating-gate NOR type 4Mb Flash test chip and confirm 100MB/s program speed by utilizing novel DSLA and SVM to the chip.

Test Chip Specifications

Target specifications of the test chip have been set to achieve 100MB/s programming speed. The page size is 2KB, the programming-pulse-period is 2.5us, the program-verify-period is 2.5us, and the iterative number of programming cycle is four. So that the total 2KB page program time is 20us, which can achieve 100MB/s programming speed, accordingly.

A 4Mb NOR type B4-Flash test chip fabricated by 130nm CMOS triple well process is shown in Fig.1.

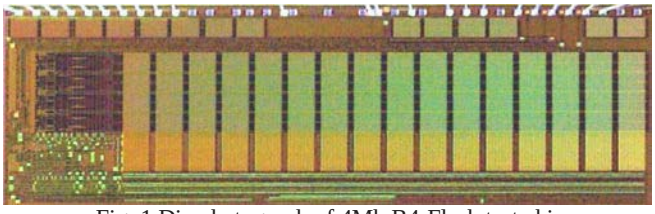

Fig. 1 Die photograph of 4Mb B4-Flash test chip.

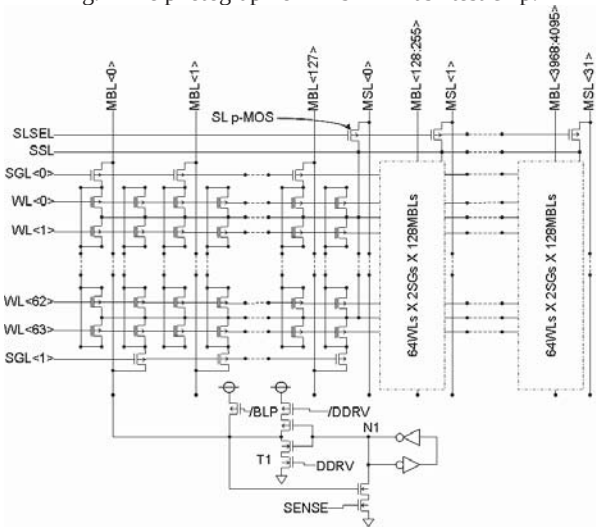

Fig. 2 Architecture of a 512Kb block.

There are eight blocks in the device. Figure 2 shows the 512Kb block architecture of the 4Mb B4-Flash test chip. Each block has 64-WLs, 4K-MBLs and two SGLs. The total number of column latch is 4K. It has one SL driver for each Sub Source Line (SSL), which is shunted by Main Source Line (MSL) via SL p-MOS in every 128-MBLs. The memory cell consists of a p-channel floating-gate device.

Programming Operation and Sequence

Programming cycle is composed of a programming-pulse-period and a program-verify-period. The programming-pulse-period consists of three periods. In the first period, the selected WL and selected Well are set to high voltage. In the second period which is drain-pulse period, the selected BLs are driven to GND while the unselected BLs are kept VCC level. In the third period, the selected WL and Well are reset to VCC level. In the drain-pulse period, B4-HEs are injected to the floating-gate of the selected cells. Figure 2 shows the schematic diagram of the column latch. In the drain-pulse period, BLs are driven to the inverted logic level of the node N1 by setting DDRV=VCC, /DDRV=GND and /BLP=VCC. "H" level of N1 corresponds that the BL is selected for programming. Figure 3 shows the measured waveforms of the programming-pulse-period. It takes 500ns to charge up the selected WL and Well. The drain-pulse period is set to 480ns. According to these results the target speed of 2.5us programming-pulse-period can be obtained.

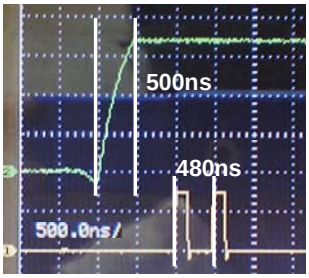

Fig. 3 Measured waveforms of programming-pulse-period.

Next subject is to achieve fast program-verify operation as described below. In the first period of program-verify operation, the selected BLs are set to GND by setting DDRV=VCC, /DDRV=GND and /BLP=VCC. In the second period, constant current of Ibias is applied to the selected BLs by changing the voltage of DDRV from VCC to Vbias which is set to certain level. The transistor T1 acts as a constant current source of Ibias. In this period, the selected WL is driven to -2V. In the third period, the program-verify operation is executed. When the cell current exceeds Ibias, the corresponding BL is charged up to indicate completion of programming. On the other hand, when it becomes lower than Ibias, the corresponding BL is set to GND level to indicate program fail. In the fourth period, each BL voltage is reloaded to the corresponding column latch by setting SENSE=VCC. The program-verify operation is executed for 4K BLs simultaneously. There is the concern that the coupling noise between neighboring BLs might cause the erratic read. Appropriate value of Ibias stabilizes BL voltage and it prevents the coupling noise effectively.

The 4Kb program-verify needs to flow up to 20mA because a current of the programmed cell is set to 5uA. In order to control the SL voltage-drop less than 100mV, the total resistance of SL must be less than 5-ohm. We have adopted the Double Source Line

Architecture (DSLA) to realize low resistance of SL. During the program-verify-period, the SSL is driven to VCC by the SL driver, and the output of SL driver is wired horizontally. In addition, SL p-MOSs are turned on so as to drive the SSL to VCC via MSLs. MSLs are located in every 128-MBLs which are wired vertically. So that one MSL shares program-verify current of 128 cells, which is independent of page size. The DSLA makes the total SL resistance low enough for any page size. According to the simulation result of 16Kb program-verify operation, the maximum voltage-drop of SL is 450mV. After 200ns, the voltage-drop becomes less than 100mV. We can recognize the efficacy of the DSLA from this simulation result.

In program-verify operation the cells which were already programmed in preceding cycle don't need to be checked. The Selective Verifying Method (SVM) is applied to verify the selected BLs. In the first period of program-verify operation, the column latch set to "0" (N1=VCC) drives the BL to GND, and the column latch set to "1" (N1=GND) drives the BL to VCC. Unnecessary operation of pre-charging to GND is omitted. In the period of the program-verify operation, the column latch set to "0" applies Ibias to the corresponding BL, and the column latch set to "1" drives the BL to VCC. This operation cuts off unnecessary bias current. Eventually SVM reduces the current consumption during the program-verify-period.

Figure 4 indicates the measured waveforms of the program-verify-period. The former trigger sets DDRV=Vbias to apply Ibias to the BLs, while the latter trigger set SENSE=VCC to reload the BL level to the column latch. The WL is driven to -2V with the same waveform as the VN which is the negative power output. It takes 720ns to select the WL and 560ns to sense cell current for program-verify respectively. These data prove that the target speeds of 2.5us program-verify is attained by using DSLA and SVM.

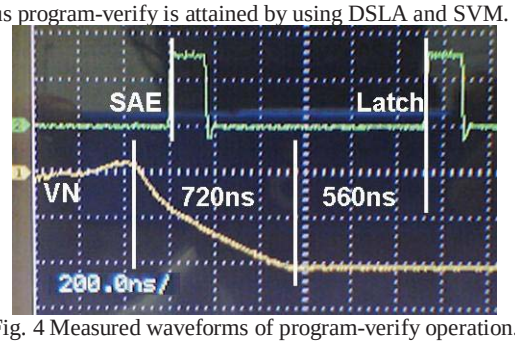

Fig. 4 Measured waveforms of program-verify operation.

Figure 5 shows the measured Vth distribution after applying 4 programming pulses. 512K bit cells (in one block) are programmed in 1.8V of Vth distribution. Each page of 4Kb cells is programmed within four program cycles. As mentioned previously, programming-pulse-period is faster than 2.5us. And the simulation result indicates 16Kb cells can be verified in 2.5us. From the results of measurement and simulation, it is estimated that 16Kb cells are programmed within 20us. Eventually, the B4-Flash can achieve 100MB/s program speed. Figure 6 demonstrates the MLC capability of B4-Flash memory with this programming method. DSLA and SVM realize three levels of programmed Vth distribution with 0.8V.

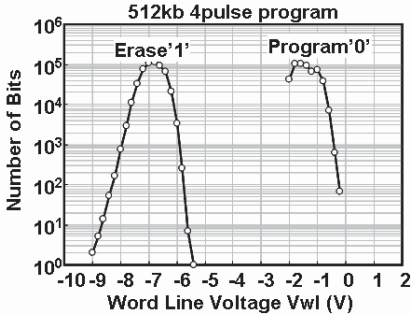

Fig. 5 Threshold voltage distributions for SLC operation.

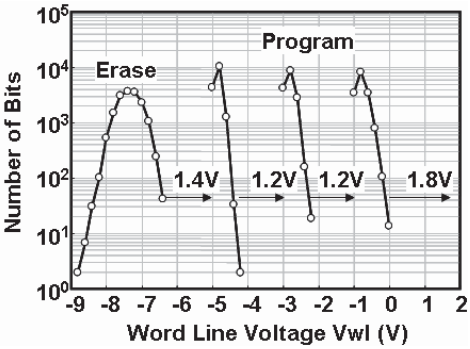

Fig. 6 Threshold voltage distributions for MLC operation.

Erase Sequence

Erase operation is done with Fowler-Nordheim (FN) tunneling as described below. SL, Well and SGLs are driven to 8V, while all the 64-WLs in the block are driven to -10V. Under this condition, SBLs are charged up to 8V via memory cells. Eventually, FN electron tunneling is carried out as an erase operation. In the erase-verify operation of conventional NOR, each cell must be verified with bit-by-bit method. On the contrary, all cells in a block are verified simultaneously in B4-Flash. The method of B4-Flash contributes to fast erase operation more than that of conventional NOR. The simultaneous erase-verify operation is as follows. All 64-WLs are set to erase-verifying voltage of -5V, and the two SGLs are set to -2.2V. The SL is set to GND although it is set to VCC for program-verify. All the BLs are set to GND by bias current. The erase-verify operation is activated by driving the SL from GND to VCC. When the erase operation is completed, all memory cells are in cut-off state, so that all the BLs are kept GND level. In case that some of the BLs are charged up to VCC, the erase operation is uncompleted. This simultaneous erase-verify operation is only applicable to the NOR type flash assigning the cut-off-cells to the erase state.

Conclusions

A 1.8V 4Mb floating-gate B4-Flash test chip has been fabricated for the first time. Novel Double Source Line Architecture (DSLA) and Selective Verifying Method (SVM), applied to NOR arrayed B4-Flash, have been confirmed to be essential and very effective to achieve 100MB/s programming speed. The MLC capability of B4-Flash memory has also been confirmed by realizing three levels of programmed Vth distribution with 0.8V width.

References

[1] K. Imamiya, et al, "A 125-mm2 1-Gb NAND Flash Memory With 10-MByte/s Program Speed" IEEE J. Solid-State Circuits, vol. 37, pp. 1493-1501, No.11 November 2002.

[2] S.Shukuri, et al., "A 60nm NOR Flash Memory Cell Technology Utilizing Back Bias Assisted Band-to-Band Tunneling Induced Hot-Electron Injection (B4-Flash)" Symp. on VLSI Technology, p.20, 2006.