Floating Gate B4-Flash Memory Technology Utilizing Novel Programming Scheme - Highly Scalable, Efficient and Temperature Independent Programming -

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Abstract

A floating gate B4-flash memory cell technology, which provides high speed programming with excellent programming efficiency for NOR architecture, has been developed. We have reported a p-channel SONOS type B4-flash cell utilizing novel Back Bias assisted Band-to-Band tunneling induced Hot-Electron(B4-HE) injection[1]. This paper demonstrates that B4-HE injection programming scheme can be easily evolved to a floating gate cell. By applying a moderate back bias to the cell during programming, the bit-line voltage can be reduced below the supply voltage, 1.8V. As a result, B4-flash can achieves high speed programming comparable to conventional NOR and high programming efficiency comparable to NAND flash at the same time. Basic operations of the floating gate B4-flash cells have been investigated. It is also confirmed that B4-HE injection programming provides very weak temperature dependency in comparison with CHE and FN injection, and does not have a negative impact to its reliability.

Introduction

The most crucial limitation in scaling of NOR flash memory cells utilizing CHE injection programming is gate length reduction. This is mainly due to the deficiency in drain to source punch-through immunity for CHE programming. So that the physical limit of the gate length is said to be around 110nm(ITRS 2006, [2]).

Another issue is its low programming efficiency in comparison with those of data storage memory such as NAND and AND, which restricts the program throughput of NOR flash comparatively low.

In this paper, we propose a p-channel floating gate B4-flash cells, in which BTBT initiated HE injection with an adequate back bias is applied for programming, same as the a p-channel SONOS device already reported[1]. It is demonstrated that B4-HE programming scheme provides not only low drain voltage programmability but also high programming efficiency comparable to NAND with very small temperature dependence and without any unexpected reliability degradation, in case of a floating gate device.

Cell Structure and Programming Characteristics

Evaluated p-channel floating gate flash memory devices(Fig.1) have been fabricated using an existing 130nm n-channel flash memory process. The channel width and gate length are 120 and 170nm, respectively. Tunnel oxide and effective inter-dielectrics thickness are 11 and 13.5nm, respectively.

The generation of B4-HEs consists of two steps, (1)BTBT generation is controlled by the vertical electric field(Vfg – Vd), (2)the generated BTBT electrons are accelerated in the depletion layer controlled by the junction electric field(Vd – Vb)(Fig.2). For the present devices an appropriate back bias(Vb) of 8.6V is quite high, however, junction breakdown is not observed even at Vb=12V(Fig.3). This is considered to be due to the reduction of effective surface potential(<Vb) by depletion layer reach through between drain and source. By modify the drain junction profile, Vb can be reduced below 5V[1]. According to the cell operation voltage(Table.1), Fig.5 shows programming and disturbs conditions in NOR array. Gate currents of programmed and three types of disturbed cells(Fig.5) are compared using floating gate contacted devices(Fig.4). Gate current of all the disturbed cells are five orders of magnitudes smaller than that of the programmed cell.

Typical programming time is about 400ns, and both disturb margins of drain and gate are about four orders of magnitudes(Fig.6) as expected from the gate current comparison, which shows the applicability of B4-HE programming to floating gate NOR architecture. Temperature dependence of B4-HE programming and Fowler-Nordheim(FN) tunneling erasure(Fig.7) show the activation energy of 5mV and 44mV, respectively. It should be noted that B4-HE injection has smaller activation energy than FN tunneling. This small activation energy of B4-HE injection can be explained by its generation process. BTBT current is in proportion to $Eg^{-0.5}$, where Eg denotes band-gap. Eg has negative temperature dependence of -0.3meV/K, so that BTBT current provides positive temperature dependence. On the other hand, hot electron generation has negative temperature dependence based on lucky electron model, because the mean-free path of the carrier has negative temperature dependence. These two mechanisms may compensate temperature dependence of B4-HE injection to achieve very small activation energy of 5mV, accordingly.

Programming drain current is around 10nA(Fig.8). Assuming 1kB word-line simultaneous programming (page program) of 128kB B4-Flash cell array (conventional erase block size of NOR), the estimated total programming current is about 100μA. As the actual programming time is estimated to be less than 10μs including verify operation, the programming throughput of 100MB/s can be achieved by utilizing 1kB page programming.

Cycling Endurance and Reliability

Estimated read disturb lifetime of the cell is extremely long(Fig.9), which is attributed to the fact that the hole impact ionization efficiency in p-channel device to be very small. Cycling endurance characteristics up to 10k cycling has been confirmed(Fig.10). High temperature data retention characteristics after 10k cycling of 128kbit cells(Fig.11) indicates that there is no fast tail-bits due to cycling. This means that B4-programing scheme does not generate the abnormal fast-charge-loss bits and there is no native drawback of the p-channel floating gate flash memory devices.

Conclusions

A floating gate B4-flash cell technology utilizing B4-HE injection for programming is proposed and successfully demonstrated by using an existing 130nm floating gate process. B4-HE programming realizes the high speed programming, comparable to conventional NOR and high programming efficiency comparable to NAND flash. It is found that B4-HE injection shows extreme small temperature dependence of Ea=5mV, which is less than that of FN tunneling. Floating gate B4-flash cell provides extremely high immunity to reading disturbance and good data retention characteristics without an unexpected abnormal fast-tail-bit. Moreover, this programming technique has a promising potential for achieving high programming throughput of 100MB/s without temperature dependence.

Acknowledgments

The authors would like to thank Prof. K.Taniguchi, Osaka University, for his support.

References

[1] S.Shukuri, et al., Symp. on VLSI Technology, p.20, 2006.
[2] G.Servalli, et al., IEDM Tech. Dig., 35_1, 2005.

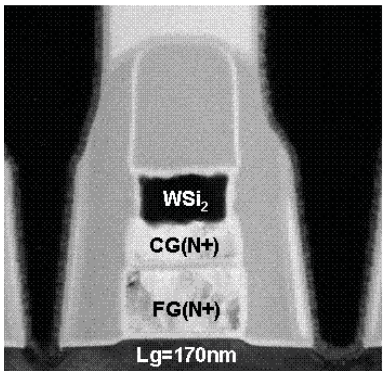


Fig.1 TEM micrograph of the cell

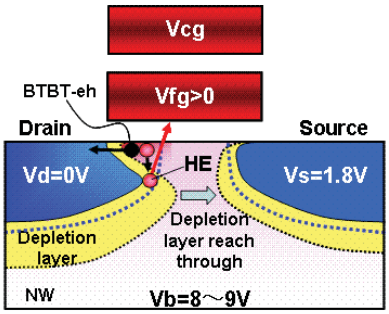


Fig.2 Back bias assisted band-to-band tunneling induced HE injection

Mode	Vcg	Vd	Vs	Vb
Program	7	0	1.8	8.6
Erase	-10	8	8	8
Read	-2	0	1.8	1.8
Stand-by	1.8	1.8	1.8	1.8

Table.1 Cell operation voltage

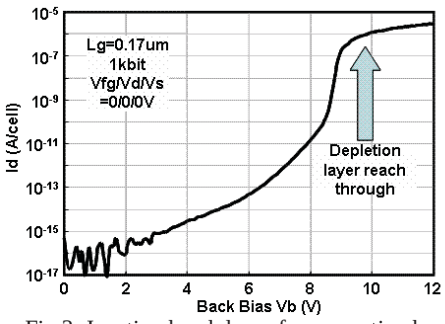


Fig.3 Junction breakdown-free operation by drain-source depletion layer reach through

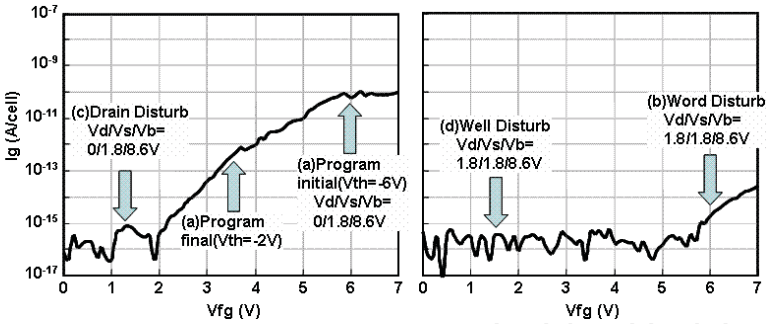


Fig.4 Gate current comparison, (a)program selected, (b)word-disturbed, (c)drain disturbed and (d)well-disturbed cells

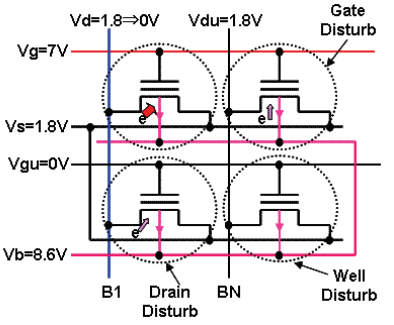


Fig.5 Program and disturb conditions in NOR array

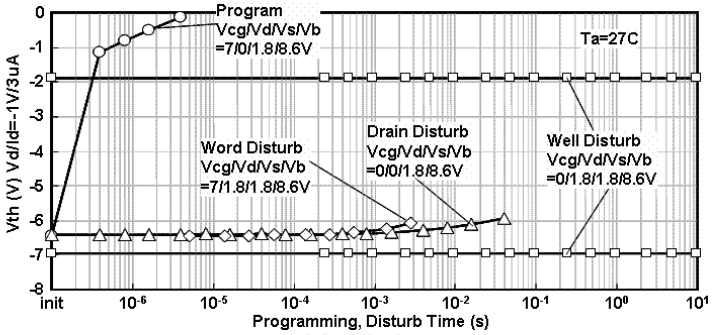
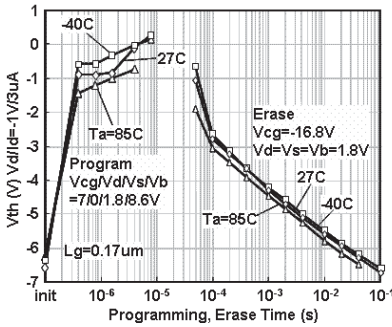


Fig.6 Program and disturb characteristics



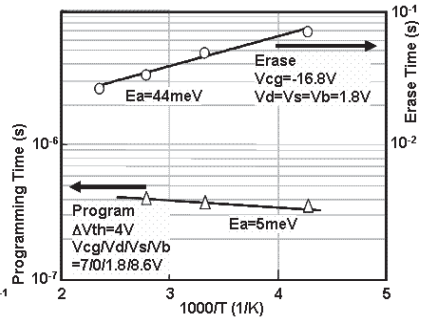


Fig.7 Temperature dependence of program and erase characteristics

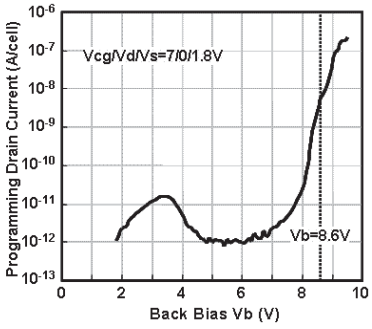


Fig.8 One-shot programming drain current

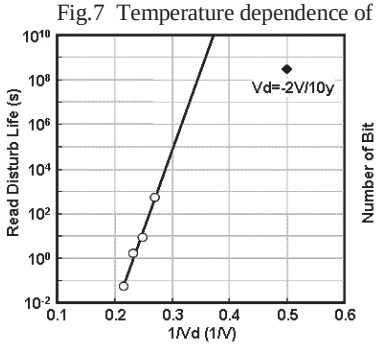


Fig.9 Read disturb lifetime

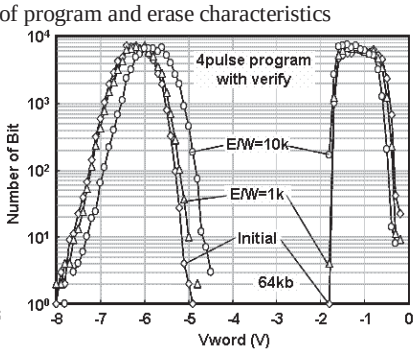


Fig.10 Cycling endurance

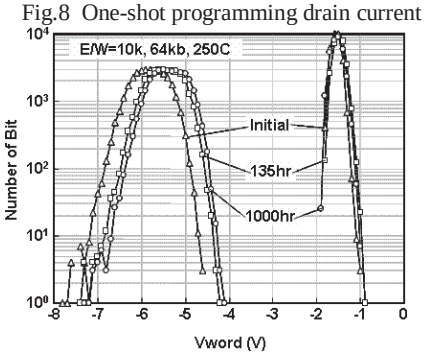


Fig.11 250C data retention after 10k cycling