A Fast Rewritable 90nm 512Mb NOR "B4-Flash" Memory with $8F^2$ Cell Size

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Abstract

This paper introduces a first 512Mb B4-Flash product chip with $8F^2$ cell size, which is the smallest NOR cell in the 90nm generation. High rewriting throughput (~8MB/s) is realized by 10MB/s programming and 100ms/block erasing without over-erase problem. 10MB/s programming is achieved by 1kB simultaneous programming and proposed fast verify scheme. This work proves that B4-Flash can realize not only high rewriting performance like NAND Flash but also fast random access like conventional NOR Flash.

Introduction

Increasing demand for high density low cost non-volatile memory applications requires fast rewriting throughput for flash memories.

We have demonstrated the high speed programming capability (100MB/s programming speed on a theoretical basis) and excellent retention characteristics of B4-Flash memory with p-channel floating gate cell by evaluating the 4Mb/64Mb test chip fabricated in 130nm/90nm process technology, respectively [1-3]. In this paper, we introduce a 90nm 512Mb B4-Flash product chip with $8F^2$ cell size for the first time, and confirm the high rewriting performance in NOR architecture practically.

Architecture

Fig. 1 shows the microphotograph and the key features of the chip. Fig. 2 shows the memory cell array architecture adopted in this chip. As have been confirmed in the previous work [4], NMOS select-transistor architecture is useful for realizing the robust program-disturb immunity (especially improving the gate-disturb immunity) in B4-Flash memory. This chip contains four 128Mb memory arrays called "BANK". 2048 write buffers for program and 256 sense amplifiers for verify and read are located in the lower side of each BANK. A block is composed of 512WL and 4096 MBL (16384 SBL), the word line pitch is 0.36um (=4F) and the bit line pitch is 0.18um (=2F) respectively, so the unit cell size is $0.0648um^2$ ($=8F^2$). The minimum page size and block size are 256B and 1MB, respectively. The 10MB/s programming is achieved by extending the page size from 256B to 1kB with simultaneous four BANKs operation. In case of the 1kB programming, the block size increases to 4MB.

Fig. 3 and Fig. 4 show the column control circuit and the timing diagram of program operation for achieving 10MB/s programming, respectively. A cell programming is executed by Back Bias assisted Band-to-Band tunneling induced Hot-Electron (B4-HE) injection mechanism. In this mechanism, programming drain current is about 10nA/cell [1], therefore 1kB simultaneous programming is available in the range of charge-pump ability (~100uA). Program-pulse for cell drain is applied through the write buffer, which decides the MBL voltage according to the programming data. Program-verify sequence is executed by using 256 SAs in each BANK, repeating eight times with changing column address in a 240ns cycle, so total verify time is about 2us.

Results and Discussion

Fig. 5(a) shows the measured waveforms during program operation. In program-pulse phase utilizing B4-HE injection mechanism, the WL voltage is increased from 6V to 11V by 1V at WELL=5V. Verify and pulse sequence is repeated in a 15us cycle within 100us, therefore 10MB/s programming (1kB/100us) can be achieved by simultaneous four BANKs operation.

Fig. 5(b) shows the measured waveforms during erase operation. In B4-Flash memory, cell in erase state turns off the current, therefore over-erase problem occurred in the conventional NOR Flash memory is negligible; accordingly erase operation can be simplified. In erase-pulse phase utilizing FN-tunneling mechanism, the WELL/SL voltage are increased from 6V to 10V by 0.2V at WL=-10V. Verify and pulse sequence is repeated within 100ms.

Fig. 5(c) shows the measured waveforms during read operation. The state of memory cell is judged by applying WL=-4V/SG=4V/SBL=0.8V, and 256SAs enables 16W page read (1st access time: 100ns, 2nd access time: 25ns).

Fig. 6 shows the Vth distributions after erase and program operation, respectively. As shown in this graph, the program-disturb bit does not exist in the physical checker pattern. It proves that NMOS select-transistor architecture has robust program-disturb immunity in B4-Flash memory.

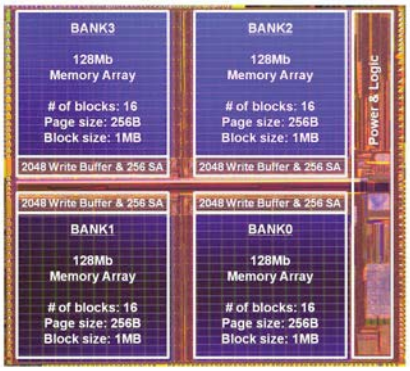
As a result, the comparison of B4-Flash memory and conventional NOR/NAND Flash memory is summarized in Fig. 7. B4-Flash memory in this work has SLC architecture, so it has 40times higher rewriting throughput (~8MB/s) than that of conventional MLC NOR Flash memory (~0.2MB/s) with fast random access which distinguishes B4-Flash memory from the serial access type of NAND Flash memory. In MLC architecture, we estimate the rewriting throughput to be 5MB/s, which can be realized by 2kB simultaneous programming within 400us and 100ms/block erasing (maximum block size: 8MB) without over-erase problem as in SLC architecture.

Conclusions

We have demonstrated the high rewriting performance of B4-Flash memory in NOR architecture practically. There is still scope for improvement of programming speed up to 20MB/s or more by extending the page size and optimizing the program sequence. In this paper, we have introduced B4-Flash memory with $8F^2$ cell size, however, it has potential to shrink a cell size down to $6F^2$ by applying a self-aligned process for contact formation. In the future, MLC NOR B4-Flash memory with high rewriting throughput and smaller cell size can be realized.

References

[1] S. Shukuri, et al., NVSMW, pp.30-31, 2007.
[2] M. Mihara, et al., NVSMW, pp.23-24, 2007.
[3] S. Shukuri, et al., NVSMW, pp.16-19, 2008.
[4] T. Ogura, et al., IMW, pp.53-54, 2009.



Process	90nm/ 3-well/ 2-poly/ 3-metal/ SA-STI CMOS
Cell size	0.18um x 0.36um = 0.0648um^2
Chip size	8.80mm x 10.19mm = 89.67mm^2
Density	512Mb (SLC)
Array	128Mb x 4BANK
Page size	256B (min.) / 1KB (max.)
Block size	1MB (min.) / 4MB (max.)
Supply voltage	1.8V (1.7V - 2.0V)
Program time	100us
Erase time	100ms
Read time	1st = 100ns, 2nd = 25ns (16W page read)

Figure 1. Die microphotograph of 512Mb B4-Flash memory

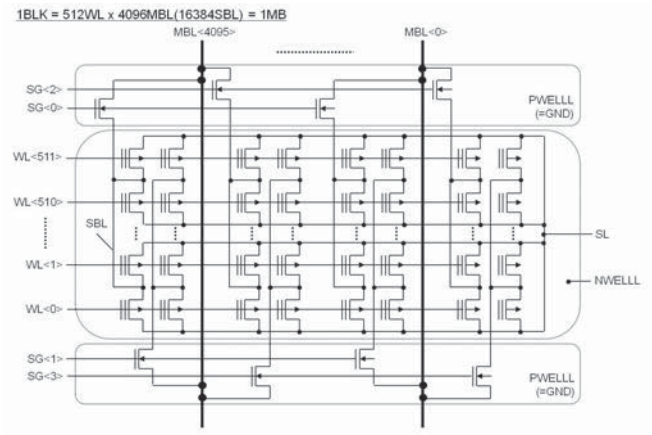


Figure 2. Memory cell array architecture

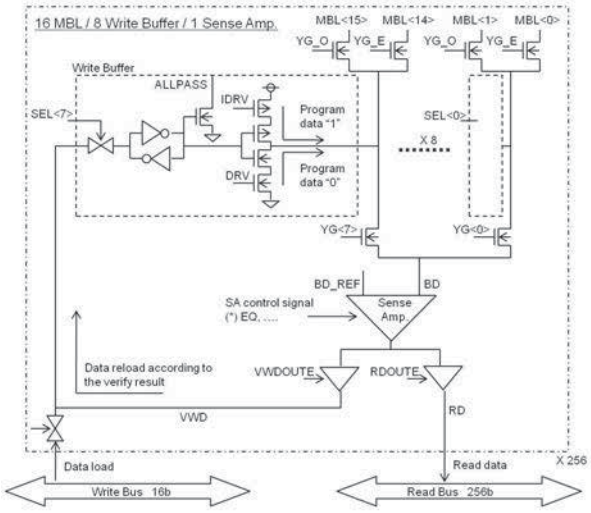


Figure 3. Column control circuit

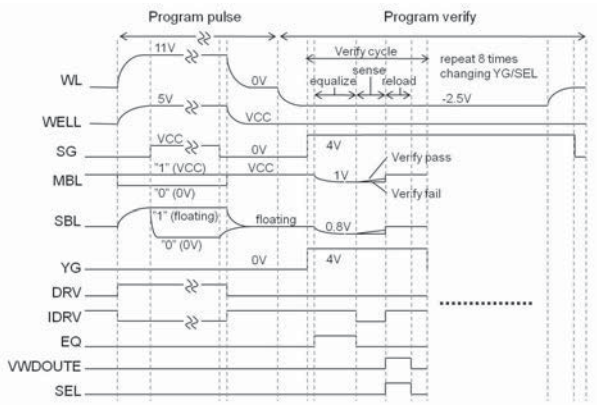
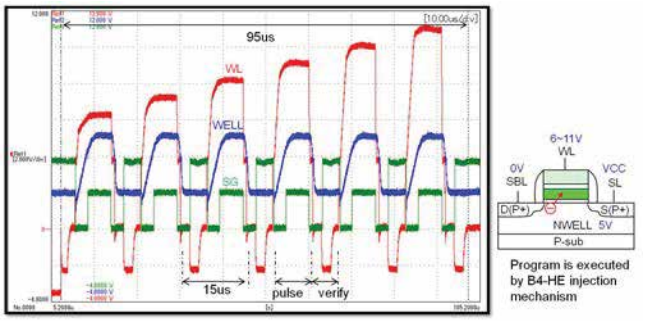
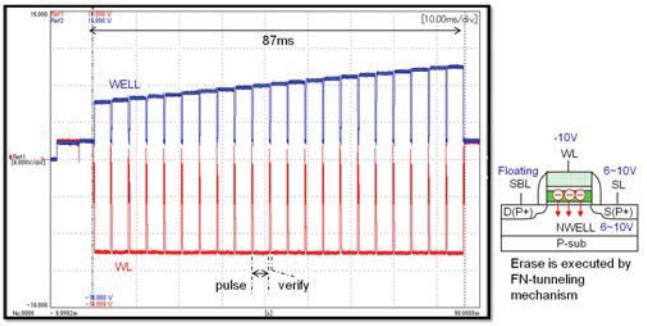


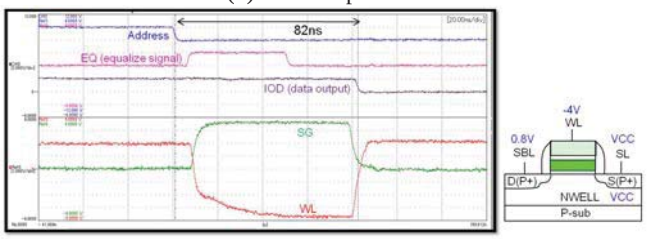
Figure 4. Timing diagram of program operation



(a) Program operation



(b) Erase operation



(c) Read operation

Figure 5. Measured waveforms

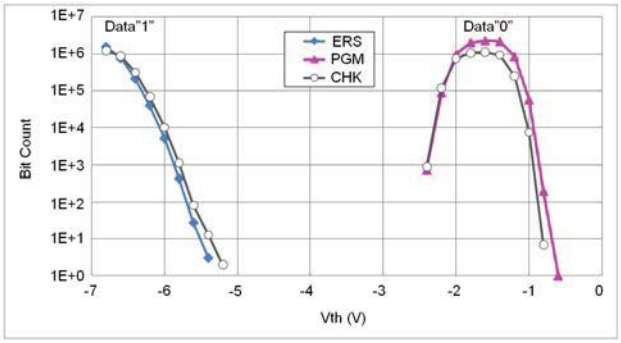
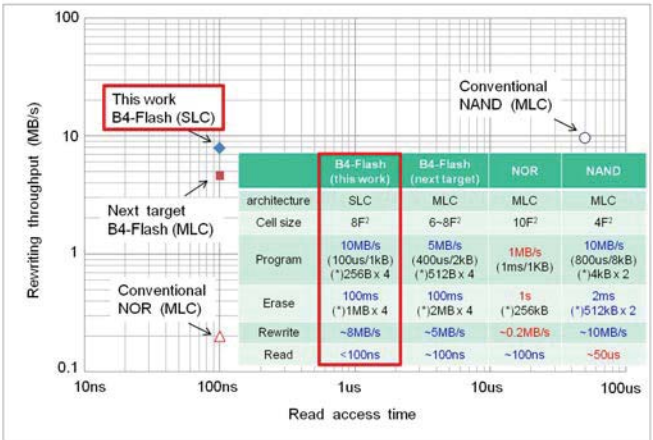


Figure 6. Vth distributions (one block = 1MB)



	B4-Flash (this work)	B4-Flash (next target)	NOR	NAND
architecture	SLC	MLC	MLC	MLC
Cell size	8F^2	6~8F^2	10F^2	4F^2
Program	10MB/s (100us/1kB) (*)256B x 4	5MB/s (400us/2kB) (*)512B x 4	1MB/s (1ms/1KB)	10MB/s (800us/8kB) (*)4kB x 2
Erase	100ms (*)1MB x 4	100ms (*)2MB x 4	1s (*)256kB	2ms (*)512kB x 2
Rewrite	~8MB/s	~5MB/s	~0.2MB/s	~10MB/s
Read	<100ns	~100ns	~100ns	~50us

Figure 7. Comparison of B4-Flash memory and conventional NOR/NAND Flash memory