A 90nm Floating Gate "B4-Flash" Memory Technology
- Breakthrough of the Gate Length Limitation on NOR Flash Memory -

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Abstract

A 90nm floating gate NOR B4-Flash memory with 1F (F: minimum feature size) gate length cell has been investigated by using 64Mbit test chip to evaluate the scalability of B4-Flash memory. 90nm (=1F) gate length of memory cell is shortest in many NOR flash memories reported previously. Basic program and erase characteristics and robust program disturb immunity of B4-Flash memory utilizing NMOS select transistor in memory cell array have been demonstrated. Furthermore, to simplify the peripheral circuits and reduce a die size, a new charge pump circuit which can generate both positive and negative high voltage at a supply voltage of 1.8V has been introduced.

Introduction

The most crucial limitation in scaling of NMOS NOR flash memory cell utilizing CHE injection programming is gate length reduction. This is mainly due to the deficiency in drain to source punch-through immunity for CHE injection programming. Therefore the physical limit of the gate length is said to be around 110nm (ITRS 2006, [1]).

We have evaluated SONOS B4-Flash memory single element with 60nm gate length and proved its promising scalability [2]. Then we have confirmed the high speed programming capability and excellent retention characteristics of floating gate NOR B4-Flash memory with 170nm gate length cell in 4Mbit test chip fabricated in a 130nm process technology [3][4][5].

In this paper, a floating gate NOR B4-Flash memory with 90nm (=1F) gate length cell has been investigated to evaluate its scalability. The operation of memory cell array has been evaluated by using 64Mbit test chip. Furthermore peripheral circuits for B4-Flash memory have been considered in detail; above all, a new charge pump circuit which can reduce the area penalty of peripheral circuits has been introduced.

Memory Cell Array Architecture

Fig. 1 is a microphotograph of 64Mbit B4-Flash memory test chip fabricated in a 90nm process technology. Memory mat is divided into 64 blocks, each block size is 1Mbit. 2048 write drivers for program and 256 sense amplifiers for verify and read are located in the lower side of memory mat.

Fig. 2 shows the schematic layout of 90nm B4-Flash memory cell and cross section of memory cell array parallel to the bit line. The word line pitch is 0.36um (=4F) and the bit line pitch is 0.18um (=2F) respectively, so the unit cell size is 0.0648um^2 (=8F^2). The gate length of memory cell is just 90nm (=1F).

Fig. 3 shows the memory cell array architecture adopted in this test chip. Each MBL is connected to one of four SBLs through the respective NMOS select transistors. NMOS select transistors are located in PWELL region between the NWELL regions of adjacent blocks.

Table 1 shows the program and erase operation conditions. Program operation is executed by Back Bias assisted Band-to-Band tunneling induced Hot-Electron (B4-HE) injection in drain side of a memory cell. During program operation, there are two program disturb modes, GD (Gate Disturb) and DD (Drain Disturb). In NMOS select transistor architecture, all select transistors connected to program inhibited cells in GD stress condition are OFF-state, so that all the SBLs are floating except for the SBL at programming "0". The floating SBLs are coupled to NWELL applied to 6V, so GD stress condition can be extremely relieved. Erase operation is executed by Fowler-Nordheim (FN) tunneling in all channel area of memory cell. As shown in this table, the voltage between SBL and SL in any operation mode is VCC or less, therefore it is easy for B4-Flash memory to shrink the gate length of memory cell.

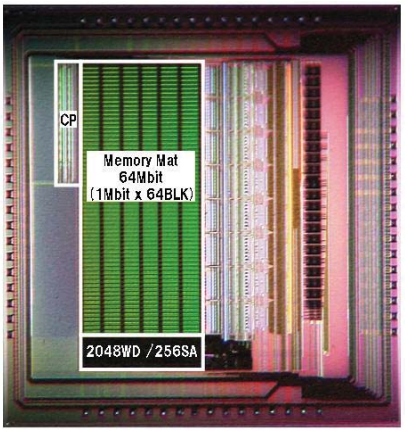

Figure 1. Microphotograph of 64Mbit B4-Flash memory test chip

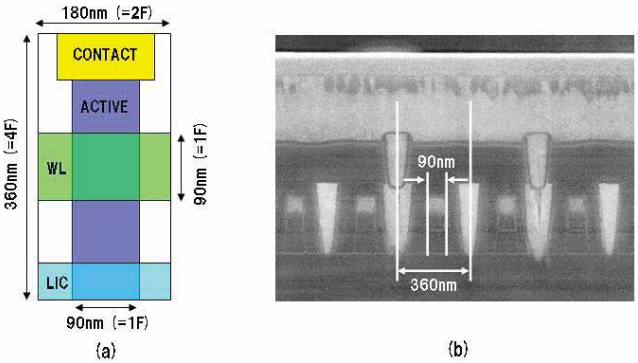

Figure 2. (a) Schematic layout of 90nm B4-Flash memory cell and (b) Cross section of the memory cell array parallel to the bit line

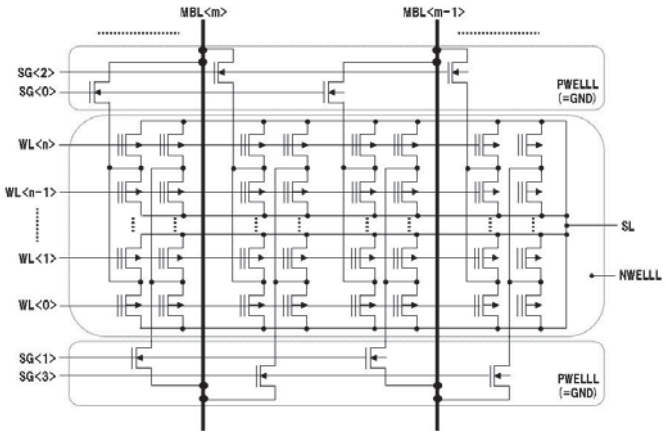

Figure 3. Memory cell array architecture

Table 1. Program and erase operation conditions

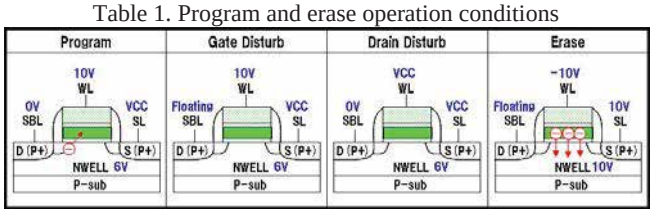

Fig. 4 shows the basic program and erase characteristics of 90nm gate length cell. Vth shifts of larger than 5V are observed with programming at WL = 10V / NWELL = 6V for 10us and erasing at WL = -10V / NWELL = 10V for 100ms respectively. Vth distributions per one block after programming and erasing are shown in Fig. 5.

Fig. 6 shows the gate and drain disturb characteristics. Both disturb margins are about 4 orders of magnitudes; it proves that NMOS select transistor architecture has robust program disturb immunity.

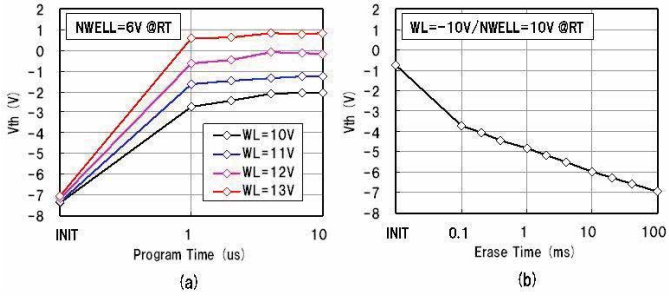

Figure 4. (a) Program characteristic and (b) Erase characteristic

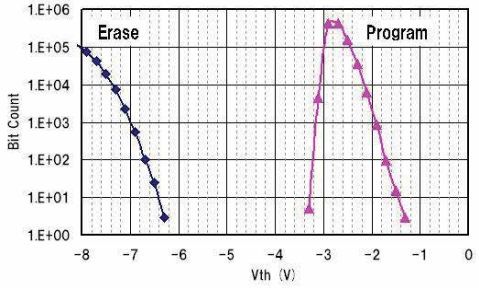

Figure 5. Vth distributions (one block = 1Mbit)

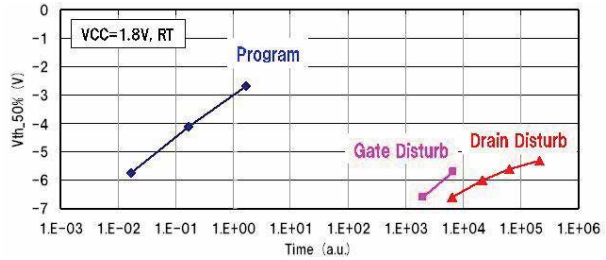

Figure 6. Gate and drain disturb characteristics

Peripheral Circuits

As mentioned above, both positive and negative high voltage are indispensable for program and erase operation in B4-Flash memory like NMOS NOR flash memory. Table 2 shows the practical combination of charge pump circuits in product chip. In the conventional architecture, two positive charge pump circuits CP_VP1&CP_VP2 and one negative charge pump circuit CP_VN are necessary, though CP_VP2 is used for program operation only, and CP_VN is used for erase operation only. In the proposed architecture, CP_VP2 and CP_VN are merged into CP_VPN to reduce charge pump circuits. CP_VPN is a charge pump circuit which can generate both positive and negative high voltage according to operation mode.

The schematic and operation mode of proposed charge pump circuit are summarized in Fig. 7. In case of positive high voltage VP output, node DNW in each stage is connected to node IN through P1 not to turn D1&D2 on, and positive high voltage is outputted to node VP through SW2. On the other hand, in case of negative high voltage VN output, node DNW is set to 0V by N3 not to turn D1&D2 on, and negative high voltage is outputted to node VN through SW1.

Fig. 8 shows the measured results of proposed charge pump circuit. +10V for VP output and -10V for VN output are adequately generated at a supply voltage of 1.8V respectively.

In this way, one charge pump circuit plays two roles, generating both positive and negative high voltage according to operation mode. It can contribute to reducing the area penalty of peripheral circuits.

Table 2. Combination of charge pump circuits

Conventional

	PGM	ERS
CP_VP1	NWELL (6V)	NWELL (10V)
CP_VP2	WL (10V)	-
CP_VN	-	WL (-10V)

Proposed

	PGM	ERS
CP_VP	NWELL (6V)	NWELL (10V)
CP_VPN	WL (10V)	WL (-10V)

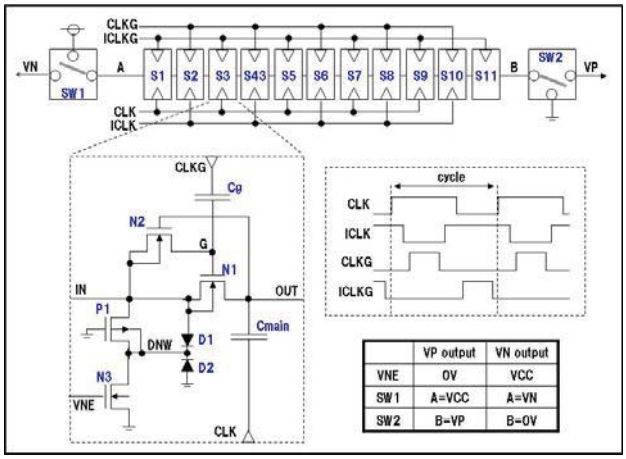

Figure 7. Proposed charge pump circuit

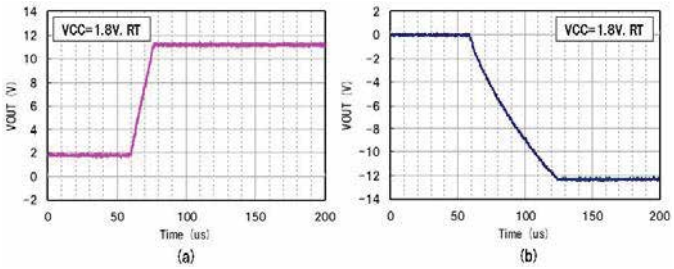

Figure 8. Measured results of charge pump circuit
(a) VP output and (b) VN output

Conclusions

We have demonstrated the scalability of B4-Flash memory by evaluating a 64Mbit test chip with 90nm (=1F) gate length cell. The basic program and erase characteristics and robust program disturb immunity of B4-Flash memory adopting NMOS select transistor architecture have been confirmed. In this test chip, we have evaluated not only the scalability of B4-Flash memory but also the reduction of peripheral circuits for product chip. A charge pump circuit which can generate both positive and negative high voltage according to operation mode is useful for simplifying the peripheral circuits and reducing a die size.

In this paper, we have introduced B4-Flash memory with $8F^2$ cell size, without using any special process for contact formation. However, B4-Flash memory has potential to shrink a cell size down to $5F^2$ by applying a self-aligned process to the bit line contact and source line LIC formation.

References

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