A 10k-Cycling Reliable 90nm Logic NVM "eCFlash"(embedded CMOS Flash) Technology

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Abstract **– This paper describes a 90nm Logic NVM "eCFlash", which can be embedded in standard CMOS process without any mask adder and any process modification. In the eCFlash element, the charge is stored in the side spacer region of CMOS transistor, consequently its charge loss process is not influenced by the leakage current through the gate oxide and surface leakage current on the side spacer, which is the most serious charge loss issues of the conventional single poly type floating gate NVM. It is shown that the intrinsic retention capability of 90nm eCFlash element is more than 10 years at 125C after 10k cycling.**

Introduction

The capability of implementing a small density electrically programmable and erasable read only memory (EEPROM) on logic products without any mask adder is strongly required for a number of applications such as redundancy implementation in SRAM, die identification, function selection, ad so on. To meet these requirements, several kinds of single poly flash memory cells have been proposed[1]-[4]. In the leading-edge CMOS, however, these cells cannot keep sufficient data retention reliability, because the gate oxide thickness becomes thinner than 8nm that is thought to be critical thickness for SILC (Stress Induced Leakage Current)[5].

Another practical issue in data retention is the fact that the leakage current between gate and diffusions easily occurs through the surface of the nitride layer for etching stopper, especially in the leading-edge CMOS process. This surface leakage current, which is the fatal origin of charge loss in the single poly NVM, tends to increase in the salicide structure, and strongly depends on stoichiometry of the nitride film. Therefore, it is difficult to control without optimization of the deposition process in the already established CMOS technology.

As an unique technical candidate, we have reported a 16k-bit 0.25um eCFlash array operation with a differential sense-latch type cell architecture[6], in which the side spacer was employed as a storage node instead of floating poly.

In this paper, a 90nm eCFlash, which can be easily embedded in standard CMOS process without any mask adder and any process modification, is demonstrated. 10k cycling capability and 125C-10years retention lifetime of the 90nm eCFlash element will be presented.

eCFlash Element and Operation

N-channel eCFlash single NVM elements have been fabricated in a 90nm CMOS process without any mask adder and any process change. In a differential sense-latch type cell architecture[6](Fig.1), two NVM elements are implemented, in which the required Vt difference between two elements for read operation is only 50mV[6]. In this architecture, moreover, read condition is identical to the Vcc transistor conventional operation, which means the read disturb immunity of eCFlash element is identical to the hot carrier life time of CMOS transistors. So that eCFlash is immune to 10 years continuous read.

The eCFlash element has an asymmetrical LDD structure(Fig.2), which consists of a I/O transistor in a 90nm CMOS logic. The source diffusion structure has been optimized for channel hot-electron(CHE) injection to the side spacer for programming and avalanche hot-hole(AHH) injection for erasure without mask adder and any process change. Read operation is achieved by applying 1V to the drain, according to a differential sense-latch type cell. Data retention test after 10k E/W cycling has been carried out at 100C, 150C, 200C and 250C up to 800hrs.

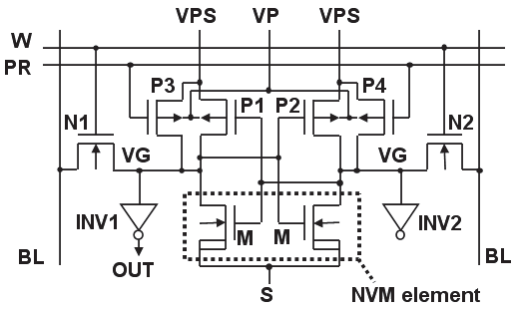

Fig.1 eCFlash cell architecture[6].

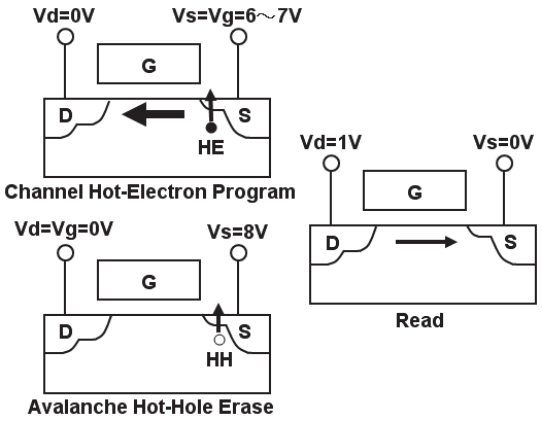

Fig.2 eCFlash element structure and its operation.

Program, Erase and Cycling Characteristics

Breakdown voltage of gate oxide and source junction is higher than 9V(Fig.3), because the NVM elements consists of I/O transistor for 5V operation. Therefore, the maximum operation voltage of 9V can be applied for programming and erase. Programming time of the W/L=0.3/0.6um element is

100ms at Vg=7V, Vs=6V, and erase time at Vs=8V is around 1s(Fig.4). In case of W/L=0.3/0.6um, programming current is 480uA/element, and erase current is 0.3nA/element. Programming time can be reduced below 10ms by increasing of channel current for CHE programming from 480uA to 600uA by shortening gate length from 0.6um to 0.4um.

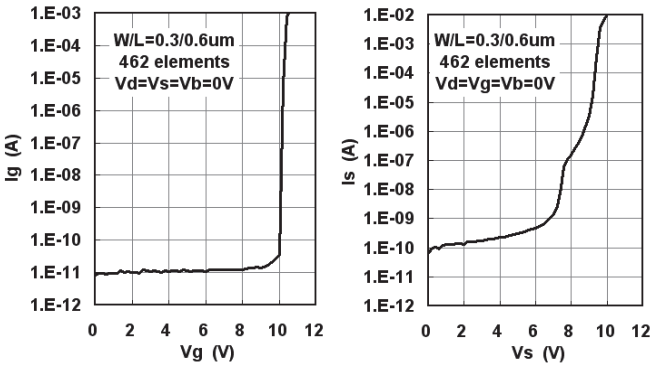

Fig.3 Gate oxide breakdown and source junction breakdown characteristics of eCFlash array with 462 elements.

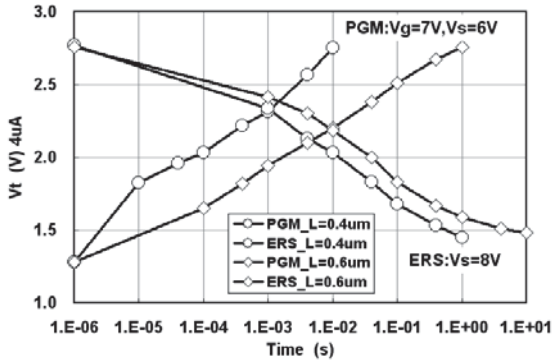

Fig.4 Program/erase characteristics.

In program/erase cycling characteristics, Both program and erase Vt rise monotonously with an increase in cycling(Fig.5). This is attributed to the fact that the injected holes by erase cannot compensate the electrons completely, because the program/erase injection positions are different. The Vt difference between the state of program and erase maintains 1V up to 10k cycling. Id-Vg curves after 10k cycling show proper subthreshold characteristics, which is sufficient for reading operation under the gate voltage between 1.5V and 4V.

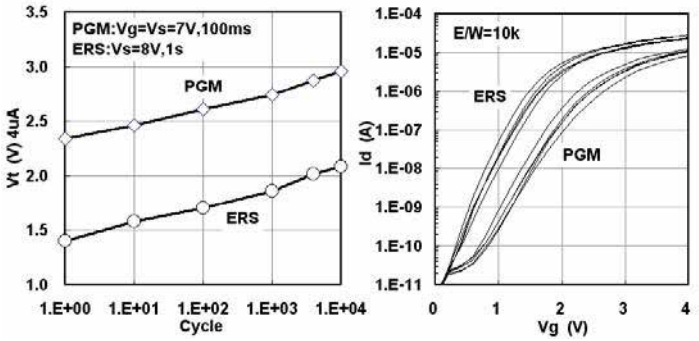

Fig.5 Program/erase cycling endurance and Id-Vg characteristics after 10k cycling.

Retrention Characteris

Initial data for retention test of eCFlash array after cycling is checker pattern. In a typical retention characteristics at 150C, Vt difference between programmed and erased state, DVt = Vtp – Vte, has been pursued(Fig.6). Both Vtp and Vte decreases proportionally to the logarithm of time, except in the early stage within one hour. This initial stage is considered to be related to the electron detrapping from the interfacial traps in the bottom oxide under Si3N4 side spacer. Long term Vt variations in both Vtp and Vte are thought to be originated by recombination of the trapped electrons and holes in the side spacer.

In eCFlash elements the charge is stored in the insulating nitride layer, so the charge loss is not influenced by leakage current through the gate oxide and surface leakage current, consequently the fast-Vt-dropping-bit frequently seen in the floating gate type NVM is hardly found.

Vt drop within one hour shows temperature dependence obviously, which becomes larger at higher temperature (Fig.7(a)), because detrapping process has a large activation energy. After initial stage, DVt decreases proportionally to the logarithm of time. Therefore, the retention lifetime can be estimated by a straight extrapolation in logarithm of time (Fig.7(b)). Retention lifetime was defined as time when DVt reached 50mV.

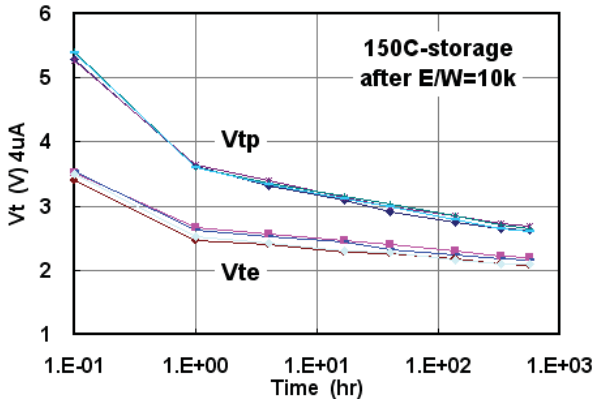

Fig. 6 Typical data retention characteristics at 150C after 10k cycling, using 10 elements.

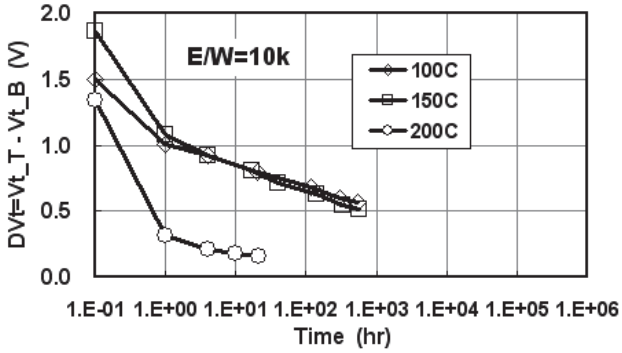

Fig.7(a) Temperature dependence of data retention characteristics after 10k cycling.

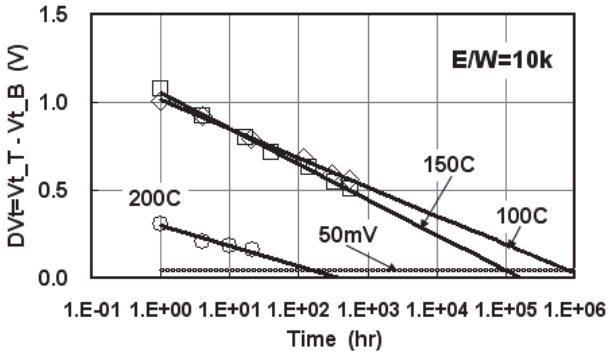

Fig.7(b) Retention lifetime estimation by straight extrapolation in the logarithm of time. Lifetime was defined as time when DVt reached 50mV.

Intrinsic retention lifetime of eCFlash element shows a remarkable cycling dependence(Fig.8). At below 10 cycling, the retention lifetime at 125C seems to be astronomical number. Increasing of cycling reduces lifetime rapidly, however, the intrinsic lifetime of 16years-125C of the 10k-cycled element can be expected.

It should be noted that the activation energy of retention lifetime also indicates strong dependency of number of cycling. Activation energy of the lifetime in the 10k-cycled element is 1.3eV. At below 10 cycling, activation energies are quite large, which might have to be approximated by the thermionic emission model[7] for lateral hopping of trapped electrons.

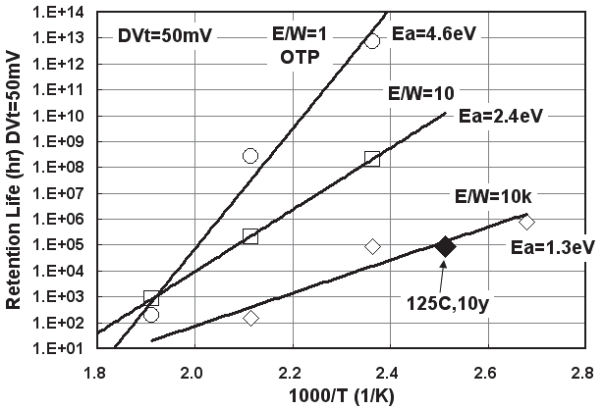

Fig.8 Cycle dependencies of Arrhenius plots of retention lifetime.

Degradation of intrinsic retention lifetime at 100C by increasing of cycling from 10k to 100k is unexpectedly small. (Fig.9). Increasing of cycling enlarges the decreasing rate of DVt, however, the initial DVt also becomes larger by the increasing of the number of excess trapped electrons, resulted in the similar lifetime. Therefore, eCFlash element has the possibility to achieve 100k cycling retention capability.

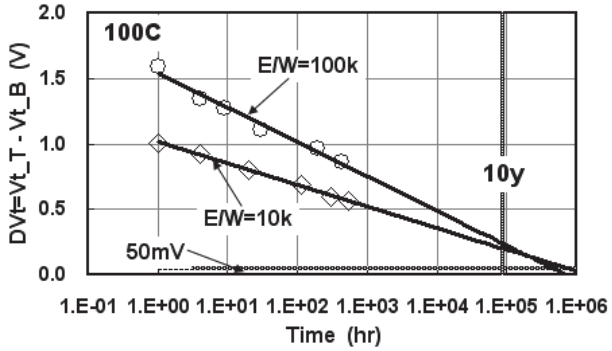

Fig.9 Comparison of 100C retention characteristics of the 100k cycled element with that of 10k cycled element.

Conclusions

A 90nm Logic NVM "eCFlash" element, which can be easily embedded in standard CMOS process without any mask adder and any process modification, was successfully developed. Excellent reliability of eCFlash element, more than 10 years retention lifetime at 125C after 10k-cycling, has been demonstrated in a 90nm CMOS process. This eCFlash technology is the best suited logic NVM element for next generation small density code storage applications for mobile phones and automotives with high reliability.

References

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