G78FVW002KSQAC

2Gbit NOR type B4-Flash

[128M by 16bit]

Products and specifications indicated to this datasheet are subject to change by GENUSION without notice.

High reliability , high speed and high density

General Description

The GENUSIONG78FVW002KSQ is a NOR flash product of GENUSION's B4-Flash (*1) technology which enables high speed program/erase and high reliability of data retention on high density devices.
The G78FVW002KSQAC is MCP（Multi Chip Package）product which is 2-dies of 1Gbit NOR flash memory packaged in 90-balls FBGA.
*1：B4-Flash(**B**ack **B**ias assisted **B**and-to-**B**and tunneling induced Hot-Electron injection **Flash**)

Features

●Memory Density

G78FVW002KSQAC： 2G (128Mx16)bit (2CE)

●Word organization

16bit (W: Words)

●Power Supply Voltage

Core (Vcc)： 1.7V～2.0V

I/O (Vccq) ： 1.7V～2.0V
2.7V～3.6V

●Low Power Consumption

Reset	:	0.13mW (Typ.)
Stand by	:	1.8mW (Typ.)
Random Read (@5MHz)	:	103mW (Typ.)
Page Read	:	26mW (Typ.)
Program	:	63mW (Typ.)
Erase	:	58mW (Typ.)

●Ambient Operation Temperature

0℃～70℃

●Package：

90balls FBGA (ball pitch: 0.8mm):

11mm x 13mm, height (max) 1.4mm

RoHS compliant

●Page size (Read)： 16W

(Program)： 128W

512W (*2)

●Block size (Erase)： 1MW

4MW (*2)

●Access Time

(1st Access)： 200ns (max.)

(2nd Access)： 30ns (max.)

●Chip Program Time (*2, *3)：

G78FVW002KSQAC： 131sec (typ.)

●Chip Erase Time (*2, *3)：

G78FVW002KSQAC： 2sec (typ.)

*2: MBO Multi Bank Operation

*3: MCI Multi Chip Interleave

●High Reliability：

Compliant with JEDEC std. JESD47I

Data Retention： 10years @55℃
after 1K P/E Cycle

Program / Erase Cycle： 10K Cycle / Block

●Process Technology： 90nm B4-Flash

Target Application

●High density code storage for industrial equipment

●High density code storage for mobile devices

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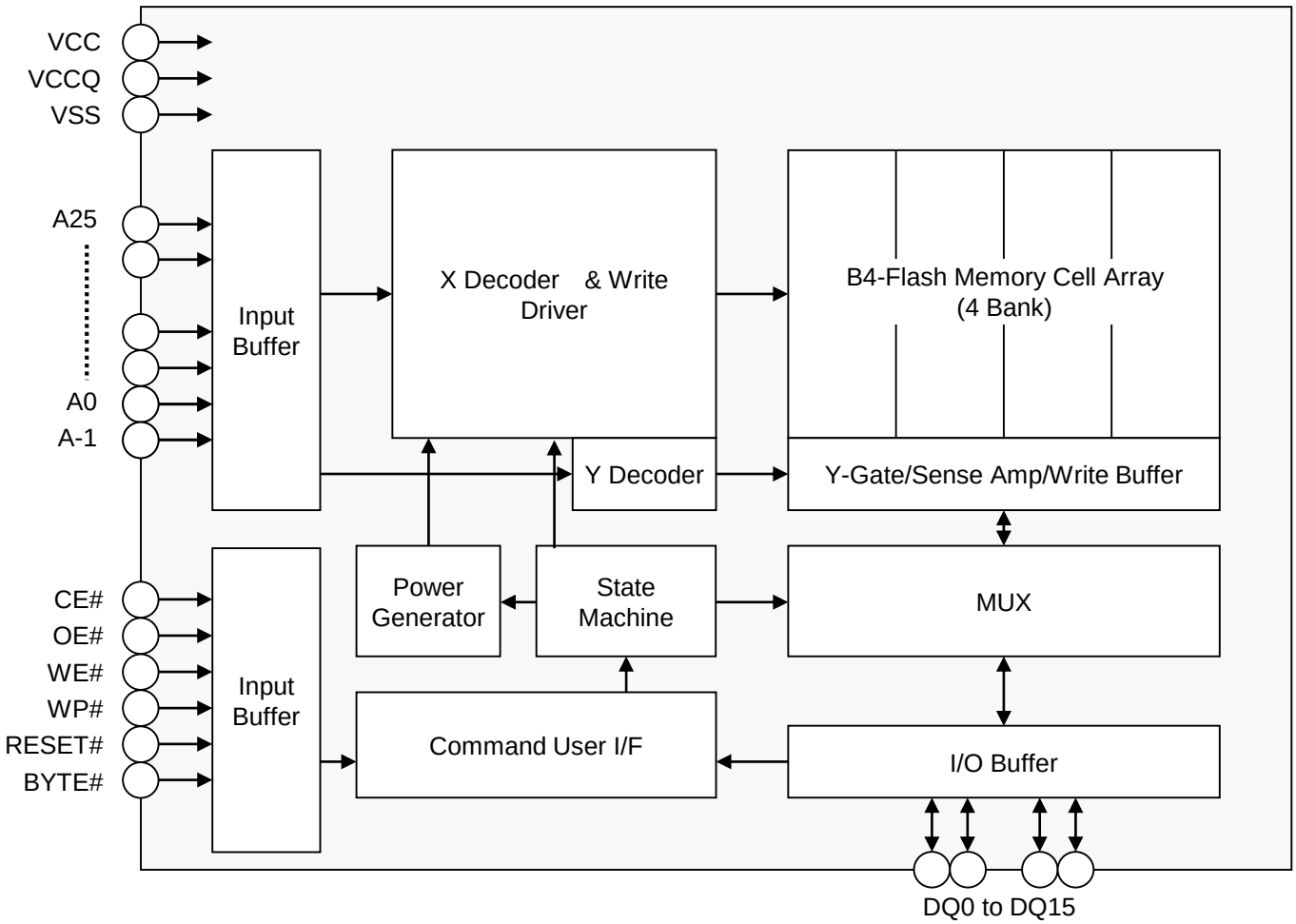
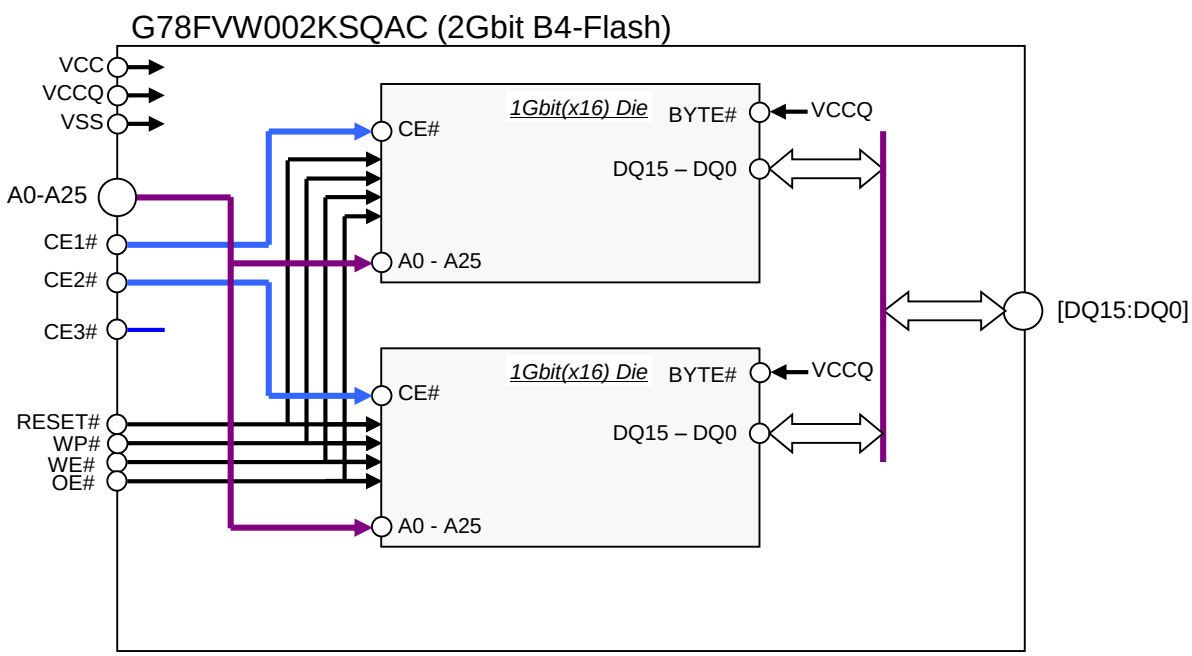
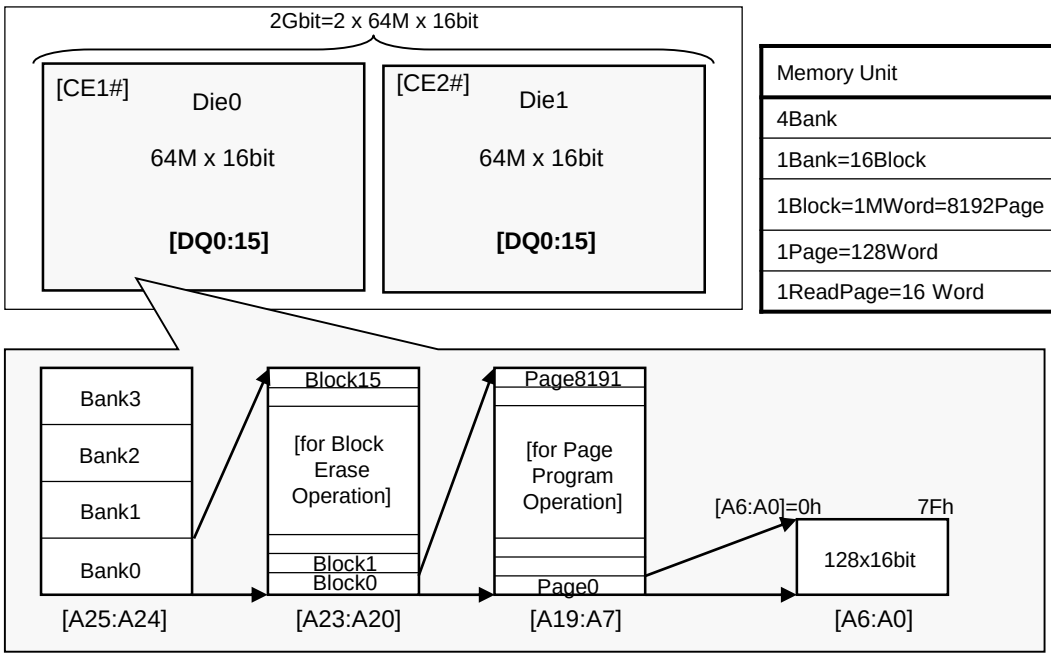
1Gbit B4-Flash Die Block Diagram



MCP(Multi-Chip Package) Block Diagram



G78FVW002KSQAC (2Gbit B4-Flash) Memory Map



Memory Unit	Address
4Bank	[A25:24]
1Bank=16Block	[A23:20]
1Block=1MWord=8192Page	[A19:7]
1Page=128Word	[A6:0]
1ReadPage=16 Word	[A3:0]

[Memory Map (CE1#="L" or CE2#="L")]

Bank / Block		Address [A0:A25]]	Size
3	63	3FFFFFFh – 3F00000h	1MW
3	62	3EFFFFFh – 3E00000h	1MW
3	61	3DFFFFFh – 3D00000h	1MW
3	60	3CFFFFFh – 3C00000h	1MW
3	59	3BFFFFFh – 3B00000h	1MW
3	58	3AFFFFFh – 3A00000h	1MW
3	57	39FFFFFh – 3900000h	1MW
3	56	38FFFFFh – 3800000h	1MW
3	55	37FFFFFh – 3700000h	1MW
3	54	36FFFFFh – 3600000h	1MW
3	53	35FFFFFh – 3500000h	1MW
3	52	34FFFFFh – 3400000h	1MW
3	51	33FFFFFh – 3300000h	1MW
3	50	32FFFFFh – 3200000h	1MW
3	49	31FFFFFh – 3100000h	1MW
3	48	30FFFFFh – 3000000h	1MW
2	47	2FFFFFFh – 2F00000h	1MW
2	46	3EFFFFFh – 2E00000h	1MW
2	45	2DFFFFFh – 2D00000h	1MW
2	44	2CFFFFFh – 2C00000h	1MW
2	43	2BFFFFFh – 2B00000h	1MW
2	42	2AFFFFFh – 2A00000h	1MW
2	41	29FFFFFh – 2900000h	1MW
2	40	28FFFFFh – 2800000h	1MW
2	39	27FFFFFh – 2700000h	1MW
2	38	26FFFFFh – 2600000h	1MW
2	37	25FFFFFh – 2500000h	1MW
2	36	24FFFFFh – 2400000h	1MW
2	35	23FFFFFh – 2300000h	1MW
2	34	22FFFFFh – 2200000h	1MW
2	33	21FFFFFh – 2100000h	1MW
2	32	20FFFFFh – 2000000h	1MW

Bank / Block		Address [A0:A25]]	Size
1	31	1FFFFFFh – 1F00000h	1MW
1	30	1EFFFFFh – 1E00000h	1MW
1	29	1DFFFFFh – 1D00000h	1MW
1	28	1CFFFFFh – 1C00000h	1MW
1	27	1BFFFFFh – 1B00000h	1MW
1	26	1AFFFFFh – 1A00000h	1MW
1	25	19FFFFFh – 1900000h	1MW
1	24	18FFFFFh – 1800000h	1MW
1	23	17FFFFFh – 1700000h	1MW
1	22	16FFFFFh – 1600000h	1MW
1	21	15FFFFFh – 1500000h	1MW
1	20	14FFFFFh – 1400000h	1MW
1	19	13FFFFFh – 1300000h	1MW
1	18	12FFFFFh – 1200000h	1MW
1	17	11FFFFFh – 1100000h	1MW
1	16	10FFFFFh – 1000000h	1MW
0	15	0FFFFFFh – 0F00000h	1MW
0	14	0EFFFFFh – 0E00000h	1MW
0	13	0DFFFFFh – 0D00000h	1MW
0	12	0CFFFFFh – 0C00000h	1MW
0	11	0BFFFFFh – 0B00000h	1MW
0	10	0AFFFFFh – 0A00000h	1MW
0	9	09FFFFFh – 0900000h	1MW
0	8	08FFFFFh – 0800000h	1MW
0	7	07FFFFFh – 0700000h	1MW
0	6	06FFFFFh – 0600000h	1MW
0	5	05FFFFFh – 0500000h	1MW
0	4	04FFFFFh – 0400000h	1MW
0	3	03FFFFFh – 0300000h	1MW
0	2	02FFFFFh – 0200000h	1MW
0	1	01FFFFFh – 0100000h	1MW
0	0	00FFFFFh – 0000000h	1MW

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G78FVW002KSQAC 90balls FBGA ball Assign(Top View)

	1	2	3	4	5	6	7	8	9	
A	A5	GND	VCCQ		Top View		VCCQ	GND	A13	A
B	A4	A18	A2				CE1#	A9	A12	B
C	A6	A0	A3				CE2#	A8	A14	C
D	A7	A1	A21				WE#	A19	A15	D
E	A17	DU	WP#				VCC	A10	A22	E
F	NC_CE3#	DU	RESET#				A20	A11	A23	F
G	DU	GNDQ	VCC				GNDQ	A25	A24	G
H	DU	DQ11	NC_DQ				DQ4	NC_DQ	A16	H
J	DQ10	DQ3	NC_DQ				DQ12	NC_DQ	NC_DQ	J
K	DQ2	NC_DQ	VCCQ				VCCQ	DQ5	NC_DQ	K
L	DQ0	NC_DQ	NC_DQ				DQ6	DQ13	NC_DQ	L
M	GND	NC_DQ	DQ9				NC_DQ	DQ7	GND	M
N	OE#	DQ8	NC_DQ				DQ14	NC_DQ	NC_A-1	N
P	VCCQ	NC_DQ	DQ1				NC_DQ	DQ15	VCCQ	P
R	GNDQ	VCCQ	GNDQ				GNDQ	VCCQ	GNDQ	R
	1	2	3	4	5	6	7	8	9	

Pin Name and Function

Symbol	Pin name	Type	Description
A<25:0>	Address	input	Address input.
DQ<15:0>	Data Input / Output	input/ output	Input of data/command for writing, output of memory/status data for reading. Or tri-state output when CEn#=“H” or OE#=“H”. Write data will be held by internal latch.
RESET#	Reset	input	By asserting RESET#=“L”, the internal operation of the flash memory will be terminated. While RESET#=“L”, input signals (address, data and other controls) are ignored. Also, during power up and down, holding RESET#=“L” prevents memory data from unexpected corruption. After changing RESET#=“H”, the flash memory exits from reset mode and becomes read mode.
CEn# (n=1,2)	Chip Enable	input	When CEn#=“L”, it enables the device selected; internal circuits and. I/Os become active. When CEn#=“H”, it disables the device and make DQ pins tri-state. Two CEn# can be selected chip in a package.
WE#	Write Enable	input	The address input signals are stored into internal latches at the falling edge of WE#, or at the falling edge of CEn# while keeping WE#=“L”. The data input signals are stored into internal latches at the rising edge of WE#, or at the rising edge of CEn# while keeping WE#=“L”.
OE#	Output Enable	input	In read mode, the pin direction of DQs become output, the data of memory or status register will be appeared on DQ pins when OE#=“L”. DQ pins become high impedance (Hi-Z) when OE#=“H”.
WP#	Write Protect	input	WP#=“L” enables the Locked Down mechanism. When WP#=“H”, overrides the Locked Down function, enabling Locked Down blocks to be Unlocked with the unlock command. After power up sequence, all blocks start from S/W locked status so that program and erase are prohibited.
VCC	Power Supply	power	Power supply for core (Flash Memory Array and Periphery logics).
VCCQ	I/O Power Supply	power	Power supply for I/O (DQ) pins.
GND	Device Ground	-	All GND pins must be connected to the System Ground.
GNDQ	Device Ground	-	Ground for I/O (DQ) pins. All GNDQ pins must be connected to the System Ground.
NC	No Connect	-	The NC pin is not internally connected to the memory device. The NC pin may be connected to one of the other signal/power lines.
DU	Don’t Use	-	The DU pin is internally connected to the memory device. It needs to be isolated from any other signal/power lines.

[Bus Interface]

Operation	RESET#	CEn#	OE#	WE#	Address	DQ
Reset	"L"	X	X	X	X	Hi-Z
Standby	"H"	"H"	X	X	X	Hi-Z
Output Disable	"H"	"L"	"H"	"H"	X	Hi-Z
Read	"H"	"L"	"L"	"H"	Valid	Dout
Write	"H"	"L"	"H"	⊓	Valid	Din
	"H"	⊔	"H"	"L"	Valid	Din

Caution: CEn# (n=1,2) must not be "L", simultaneously. When CEn#(n=1,2) is "L", CEm#(m<>n) must be remained "H".

[Read Device Information]

Device Information	Bus Status in Reading		Remarks
	Address	Word Data	
JEDEC Device Manufacturer Code	00h	XX1Ah	GENUSION
Device ID Code	01h	0000h	Device ID
Block Lock Status	Block ADD+02h	ex: DQ0=Lock Status DQ1=Lock Down Status	Also please see p15-p16
Enhanced Configuration Register	06h	ECR Data	

[Device Manufacturer Code & Device ID Code]

Command	Bus cycle	Address								Word Data	W / R
		[A25:7]	[A6:0]								
			A6	A5	A4	A3	A2	A1	A0	hex		
JEDEC Device Manufacturer Code	1	BLK	X	X	X	X	X	X	X	00h	XX90h	W
	2	X	L	L	H	H	L	L	L	18h	XX7Fh	R
	3	X	L	L	H	L	H	L	L	14h	XX7Fh	R
	4	X	L	L	H	L	L	L	L	10h	XX7Fh	R
	5	X	L	L	L	H	H	L	L	0Ch	XX7Fh	R
	6	X	L	L	L	H	L	L	L	08h	XX7Fh	R
	7	X	L	L	L	L	H	L	L	04h	XX7Fh	R
	8	X	L	L	L	L	L	L	L	00h	XX1Ah	R
Device ID Code	1	BLK	X	X	X	X	X	X	X	00h	XX90h	W
	2	X	L	L	L	L	L	L	H	01h	XX00h	R
	3	X	L	L	L	H	H	H	L	0Eh	XX00h	R
	4	X	L	L	L	H	H	H	H	0Fh	XX00h	R

(X denotes "Don't Care".)

[Status Register Definitions]

SR Bit	Name	Definitions	
[15:8]	Reserved	Reserved for Future Use. (being set to “Zero”)	
[7]	Ready Status	0	Device in Busy
		1	Device in Ready
[6]	Erase Suspend Status	0	Not in Erase Suspend
		1	In Erase Suspend
[5,4]	Command Sequence Error	00	Program and Erase operation successful
		01	Program Operation Aborted
		10	Erase Operation Aborted
		11	Command Sequence Error
[3]	Reserved	Reserved for Future Use. (being set to “Zero”)	
[2]	Program Suspend Status	0	Not in Program Suspend
		1	In Program Suspend
[1]	Block Locked Error	0	Block not Locked
		1	Block Locked / Operation aborted
[0]	Reserved	Reserved for Future Use. (being set to “Zero”)	

[Enhanced Configuration Register Definitions]

ECR Bit	Name	Definitions	
[15]	Reserved	Reserved for Future Use	
[14]	Reserved	Reserved for Future Use	
[13:3]	Reserved	Reserved for Future Use. (being set to “Zero”)	
[2:0]	Output Driver Control	001	1
		010	2
		011	3
		100	4 (default)
		101	5
		110	6
		others	Reserved for Future Use

[Output Driver Control]

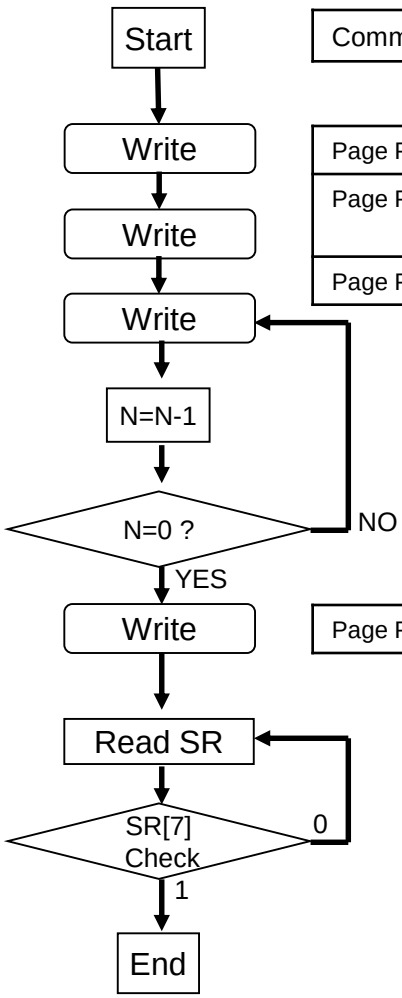
ECR [2:0]	Definitions		Output Driver Multiplier	
			VCCQ=3.3V	VCCQ=1.8V
[2:0]	001	1	1/4	1/3
	010	2	1/2	1/2
	011	3	3/4	2/3
	100	4(default)	1	1
	101	5	5/4	3/2
	110	6	3/2	2

[Command Bus Operation]

Operation Mode		Command Cycle	Command Code		Description
			Address	Data in x16	
Read	Read Array	Setup	Bank ADD	XXFFh	
	Read Status Register	Setup	Bank ADD	XX70h	
	Read Device Information	Setup	Bank ADD	XX90h	
	Read CFI Code	Setup	Bank ADD	XX98h	
Program/Erase	Page Program	Setup1 Setup2 Data Write Confirm	Start ADD Start ADD Word ADD Page ADD	XXE9h Word Count-1 Prog Data XXD0h	Program Start Add Max of Word Count=128 Repeat to 'Word Count" Confirm
	Word Program	Setup Confirm	Word ADD Word ADD	XX41h Prog Data	
	Block Erase	Setup Confirm	Block ADD Block ADD	XX20h XXD0h	
	Program/Erase Suspend	Setup Status Read Read Array	Block ADD Block ADD Block ADD	XXB0h XX70h XXFFh	 "Read Status Register" "Read Array"
	Program/Erase Resume	Setup	Block ADD	XXD0h	
Lock Block	Lock Block	Setup Confirm	Block ADD Block ADD	XX60h XX01h	
	Unlock Block	Setup Confirm	Block ADD Block ADD	XX60h XXD0h	
	Lock Down Block	Setup Confirm	Block ADD Block ADD	XX60h XX2Fh	
Register	Clear Status Register	Setup	Bank ADD	XX50h	
	Program Enhanced Configuration Register	Setup Confirm	Reg Data Reg Data	XX60h XX04h	
	Page Program User OTP	Setup1 Setup2 Data Write Confirm1 Confirm2	OTP ADD OTP ADD OTP ADD OTP ADD OTP ADD	XXC1h XX4Fh OTP Data 0000h XXD0h	OTP Entry Setup Program Data Confirm (16cycles) Confirm
	Read User OTP	Setup Exit	OTP ADD Don't Care	XXC1h XXFFh	OTP Entry OTP Exit (Normal Read)

Undefined commands must not be inputted.

(1)Page Program Flowchart



Command	Address	Word Data
Page Program Setup	Page ADD	XXE9h
Page Program Load 1	Page ADD	(N-1)h: (*1) Word Count : N
Page Program Load 2	Word ADD (*2)	Program Data
Page Program Confirm	Page ADD	XXD0h

Check SR[7]	Data
WSM Ready (*3)	1
WSM Busy (*4)	0

Before start Program operation, status register must be cleared and the block to be programmed must be confirmed as “Unlock Block” by checking Block Lock Status (p17-p18).
To start read array just after programming, Read Array command must be issued.

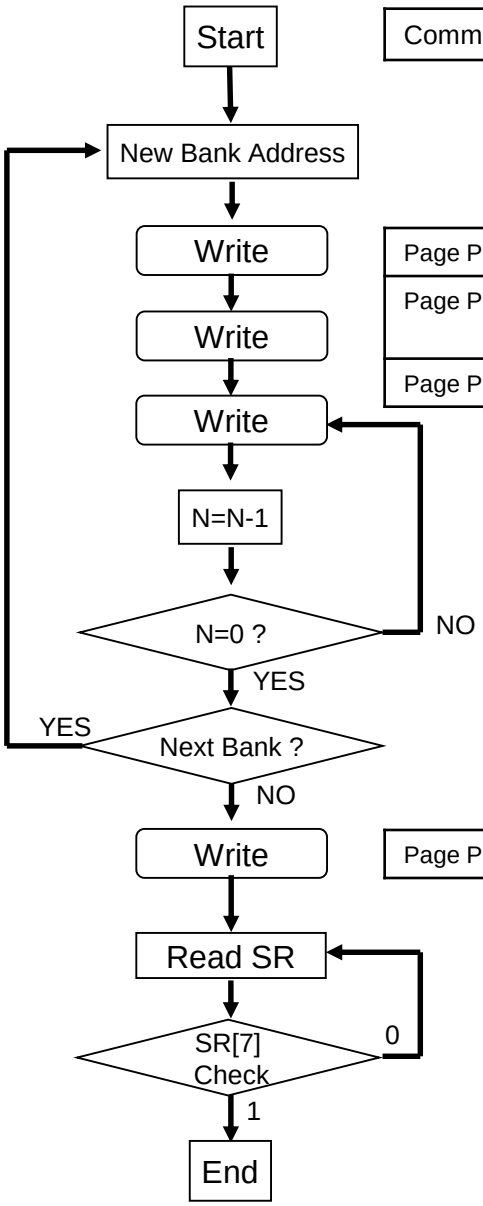
(*1):
-“Word count” indicates the number of program data in [A6:A0]. Therefore, Maximum Word Count (N) is 128, so that, Max of (N-1) = 127 = 7Fh.
-Word Count (N) must be multiple of 16, so that, program unit must be n x 16words (n=0 to 7), otherwise Program operation will be aborted as “sequence error”. Each 16words must be in address X0h to XFh (X=0 to 7) in [A6:A0].

(*2):
-Word Address in the page is to be input in [A6:A0], so that, Max. word count = 128.
-Program address must be in same page address.
- Page Program operation must be executed in proper sequence, so that a page w/A7=L must be programmed first and then, next page w/A7=H.

(*3):
-To avoid any interferences, please “power off” or “Reset” while WSM ready.

(*4):
-In a situation to shut down while SR[7]=0 (Busy), please follow the sequence shown in p.22.

(2)Multi-Bank Page Program Flowchart



Command	Address	Word Data
Page Program Setup	Bank/Page ADD	XXE9h
Page Program Load 1	Bank/Page ADD	(N-1)h: (*1) Word Count : N
Page Program Load 2	Word ADD	Program Data
Page Program Confirm	Page ADD	XXD0h

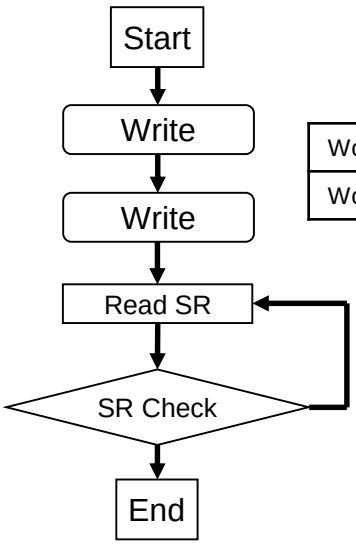
Check SR[7]	Data
WSM Ready (*3)	1
WSM Busy (*4)	0

Before start Program operation, status register must be cleared and the block to be programmed must be confirmed as “Unlock Block” by checking Block Lock Status (p15-p16).
To start read array just after programming, Read Array command must be issued.

(*1):
-“Word count” indicates the number of program data in [A6:A0]. Therefore, Maximum Word Count (N) is 128, so that, Max of (N-1) = 127 = 7Fh.
-Word Count (N) must be multiple of 16, so that, program unit must be n x 16words (n=0 to 7), otherwise Program operation will be aborted as “sequence error”. Each 16words must be in address X0h to XFh (X=0 to 7) in [A6:A0].
(*2):
-Word Address in the page is to be input in [A6:A0], so that, Max. word count = 128. - Page Program operation must be executed in proper sequence, so that a page w/A7=L must be programmed first and then, next page w/A7=H.
(*3):
-To avoid any interferences, please “power off” or “Reset” while WSM ready.
(*4):
-In a situation to shut down while SR[7]=0 (Busy), please follow the sequence shown in p.22.

(3)Word Program Flowchart

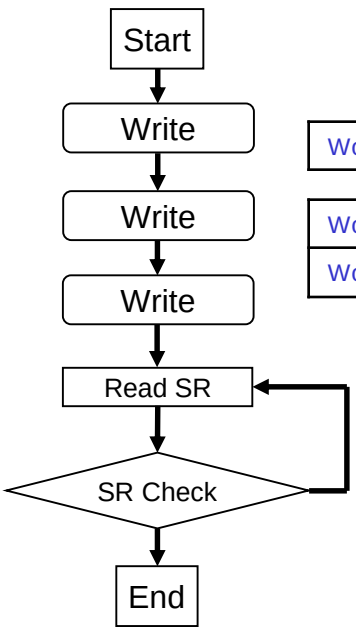
[in Word Mode (BYTE#="H")]



Word Program Setup	Word ADD	XX41h
Word Program Confirm	Word ADD	Program Data

Check SR[7]	Data
WSM Ready (*1)	1
WSM Busy (*2)	0

[in Byte Mode (BYTE#="L")]



Word Program Setup	Word ADD	XX41h

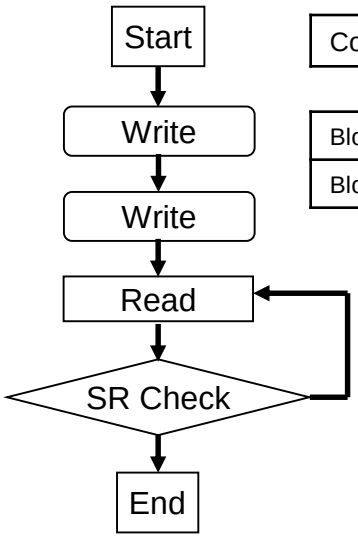
Word Program Confirm1	Byte ADD(A-1=L)	Program Data
Word Program Confirm2	Byte ADD(A-1=H)	Program Data

Check SR[7]	Data
WSM Ready (*1)	1
WSM Busy (*2)	0

- "Single Byte Program" is not supported.
- Once a "Word Program" is executed at an address of A[25:4], additional "Word Program" is prohibited in the same A[25:4] address range unless otherwise erased.

(*1):
-To avoid any interferences, please "power off" or "Reset" while WSM ready.
(*2):
-In a situation to shut down while SR[7]=0 (Busy), please follow the sequence shown in p.25.

(4)Block Erase Flowchart

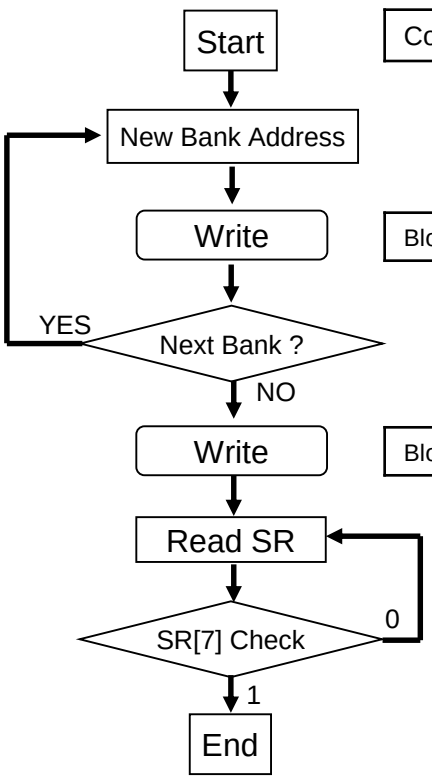


Command	Address	Word Data
Block Erase Setup	Block ADD	XX20h
Block Erase Confirm	Block ADD	XXD0h

Check SR[7]	Data
WSM Ready (*1)	1
WSM Busy (*2)	0

Before start Erase operation, status register must be cleared and the block to be erased must be confirmed as “Unlock Block” using Block Lock Status Check.
To start read array just after erasing, Read Array command must be issued.

(5)Multi-Bank Block Erase Flowchart



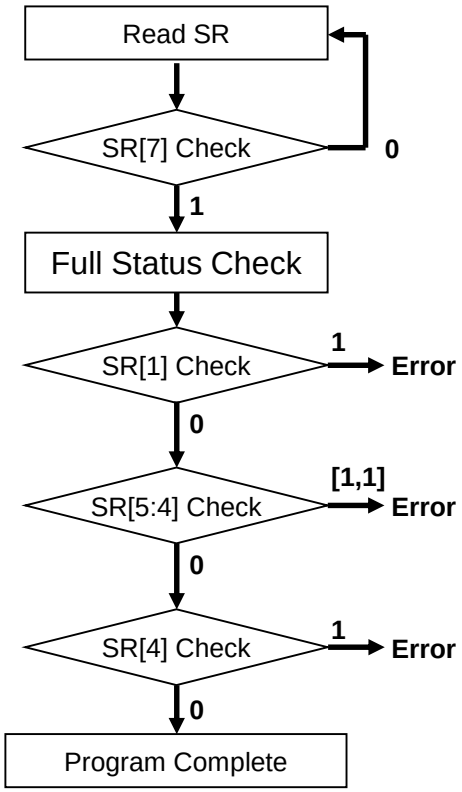
Command	Address	Word Data
Block Erase Setup	Bank/Block ADD	XX20h
Block Erase Confirm	Bank/Block ADD	XXD0h

Check SR[7]	Data
WSM Ready (*1)	1
WSM Busy (*2)	0

Before start Erase operation, status register must be cleared and the block to be erased must be confirmed as “Unlock Block” using Block Lock Status Check.
To start read array just after erasing, Read Array command must be issued.

(*1):
-To avoid any interferences, please “power off” or “Reset” while WSM ready.
(*2):
-In a situation to shut down while SR[7]=0 (Busy), please follow the sequence shown in p.25.

(6) Program Status Check Flowchart



Check SR[7]	Data
WSM Ready (*1)	1
WSM Busy (*2)	0

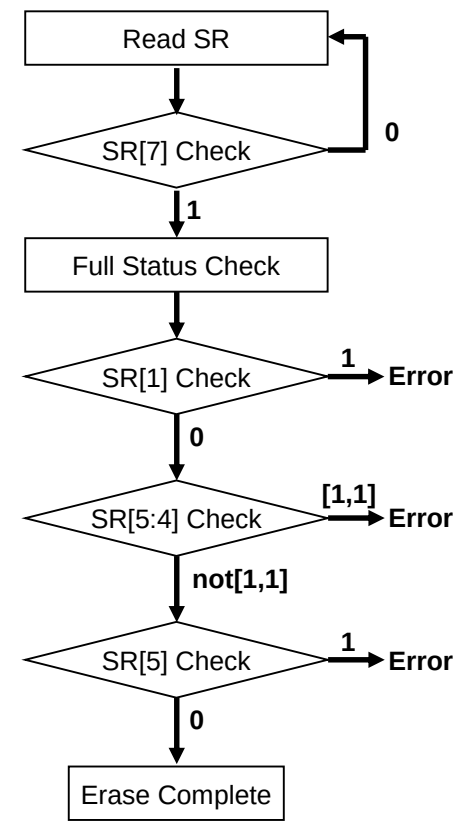
Check SR[1]	Data
Block Locked	1
Block Unlocked	0

Check SR[5:4]	Data
Sequence Error	[1,1]
Sequence OK	Not[1,1]

Check SR[4]	Data
Program Error	1
Program OK	0

If an error is detected, the Status Register should be cleared before continuous operations.
Only the Clear Status Register Command clears the Status Register error bits.

(7) Erase Status Check Flowchart



Check SR[7]	Data
WSM Ready (*1)	1
WSM Busy (*2)	0

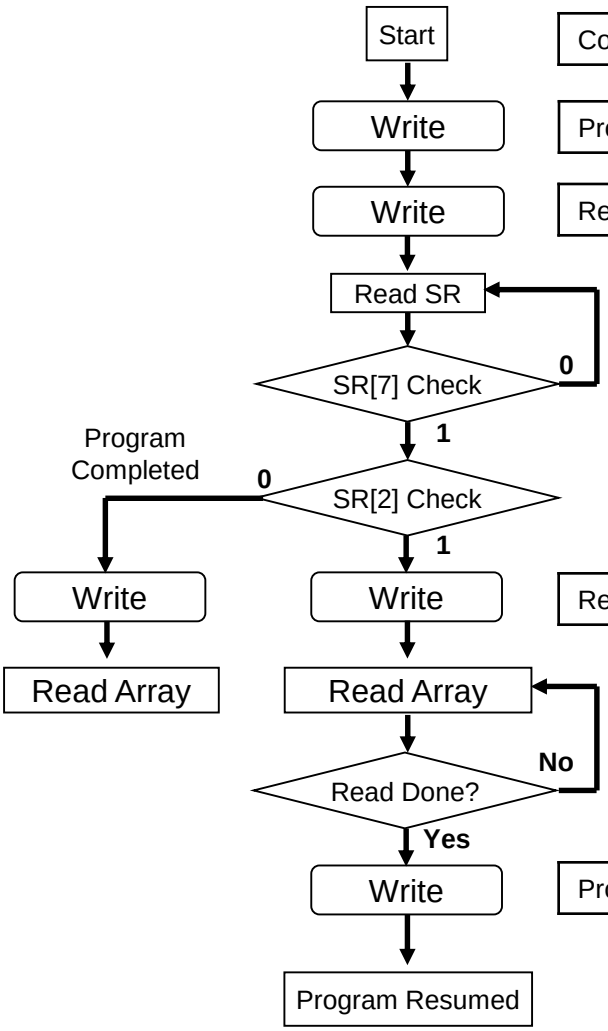
Check SR[1]	Data
Block Locked	1
Block Unlocked	0

Check SR[5:4]	Data
Sequence Error	[1,1]
Sequence OK	Not[1,1]

Check SR[5]	Data
Erase Error	1
Erase OK	0

(*1): To avoid any interferences, please “power off” or “Reset” while WSM ready.
(*2): In a situation to shut down while SR[7]=0 (Busy), please follow the sequence shown in p.25.

(8)Program Suspend, Read Array and Resume Flowchart



Command	Address	Word Data
Program Suspend	Block ADD	XXB0h
Read Status	Block ADD	XX70h

Check SR[7]	Data
WSM Ready (*1)	1
WSM Busy	0

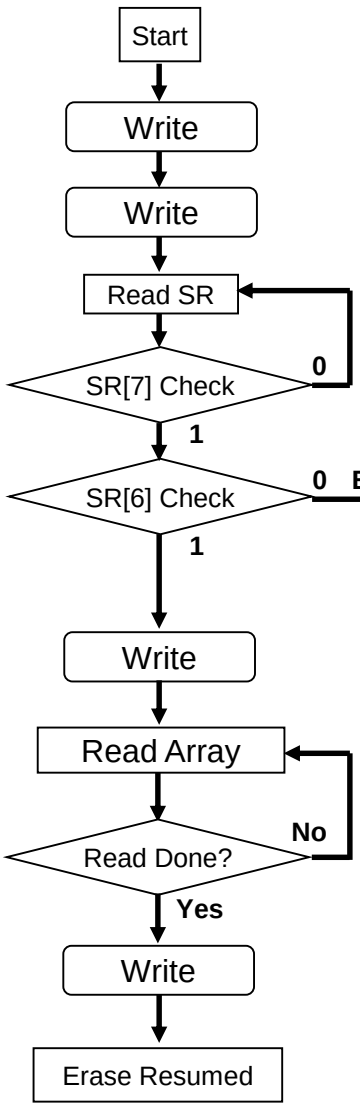
Check SR[2]	Data
Program Suspended	1
Program Completed	0

Read Array	Block ADD	XXFFh

Program Resume	Block ADD	XXD0h

(*1):
-To avoid any interferences, please “power off” or “Reset” while WSM ready.
-After suspended, device can be powered off in safety.

(9)Erase Suspend, Read Array and Resume Flowchart



Command	Address	Word Data
Erase Suspend	Block ADD	XXB0h
Read Status	Block ADD	XX70h

Check SR[7]	Data
WSM Ready (*1)	1
WSM Busy	0

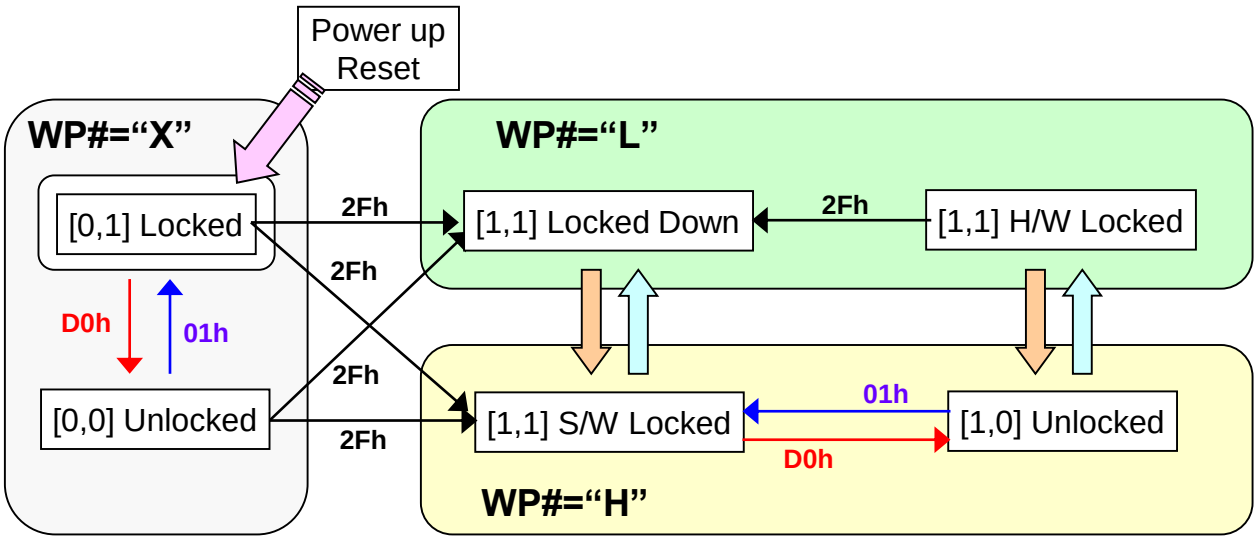
Check SR[6]	Data
Erase Suspended	1
Erase Completed	0

Read Array	Block ADD	XXFFh

Erase Resume	Block ADD	XXD0h

(*1):
-To avoid any interferences, please “power off” or “Reset” while WSM ready.
-After suspended, device can be powered off in safety.

[Block Lock Status]



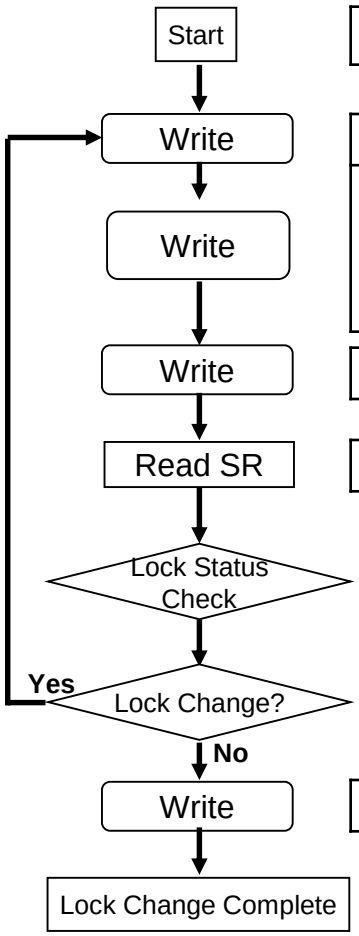
[x,x] indicates [DQ1,DQ0]

DQ0: Lock State
"1"-Lock State
"0"-Unlock State
DQ1: Lock Down State
"1"-Lock Down Select
"0"-Lock Down Unselect

mode	WP#	Lock Status Bit [DQ1,DQ0]	Locked BLK	Remarks
Lock Down	"L"	[1,1]	All Block	
H/W Locked				
S/W Locked	"H"	[1,1]	Lock Down Block	
Locked		[0,1]	Lock Block	All Block is locked after Power-Up and Reset.
Unlocked		[1,0]	Unlock Block	

Command	Setup		Confirm	
	Address	Word Data	Address	Word Data
Lock Block	Block Add	XX60h	Block Add	XX01h
Unlock Block	Block Add	XX60h	Block Add	XXD0h
Lock Down Block	Block Add	XX60h	Block Add	XX2Fh

[Block Lock/Unlock Flow Chart]



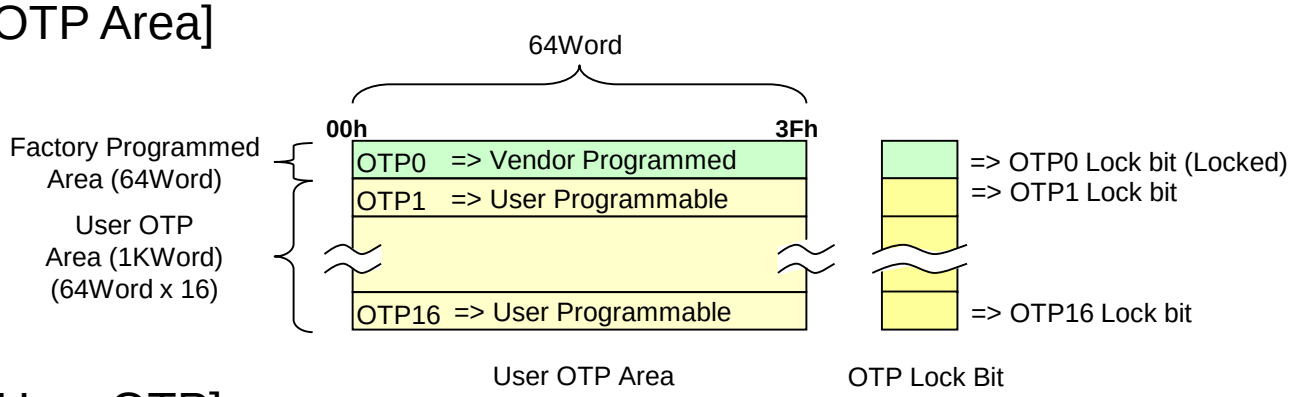
Command	Address	Word Data
Lock Block Setup	BLK ADD	XX60h
Lock Block Confirm		
<Unlock>	BLK ADD	XXD0h
<Lock>	BLK ADD	XX01h
<Lock-Down>	BLK ADD	XX2Fh
Read Device Information	BLK ADD+2h	XX90h
(Read Operation)	BLK ADD+2h	Lock Status

Check SR[1,0]	Data
Refer to Lock Status Check Table	

Read Array	BLK ADD	XXFFh

Block Lock, Lock Down and Unlock command must not be issued during “Busy” (SR[7]=0), Program suspend and Erase suspend (SR[6]or[2]=1).

[OTP Area]



[User OTP]

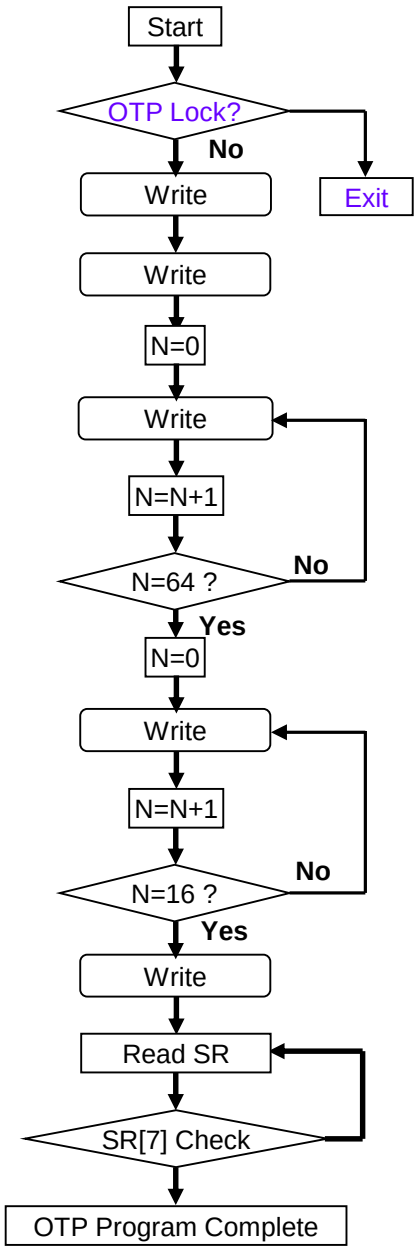
OTP Area		OTP Area Address in x16 mode									
OTP #	Function	Page Address A14-A7									Word Address
		A14	A13	A12	A11	A10	A9	A8	A7	Hex	A6-A0
OTP16	User Programmable OTP	0	0	0	0	0	0	0	0	00h	Area size : 64Word 00h-3Fh in A6 – A0 as Word Address. In User OTP area, A15-A25 will be ignored.
OTP15		0	0	0	0	1	0	0	0	08h	
OTP14		0	0	0	1	0	0	0	0	10h	
OTP13		0	0	0	1	1	0	0	0	18h	
OTP12		0	0	1	0	0	0	0	0	20h	
OTP11		0	0	1	0	1	0	0	0	28h	
OTP10		0	0	1	1	0	0	0	0	30h	
OTP09		0	0	1	1	1	0	0	0	38h	
OTP08		0	1	0	0	0	0	0	0	40h	
OTP07		0	1	0	0	1	0	0	0	48h	
OTP06		0	1	0	1	0	0	0	0	50h	
OTP05		0	1	0	1	1	0	0	0	58h	
OTP04		0	1	1	0	0	0	0	0	60h	
OTP03		0	1	1	0	1	0	0	0	68h	
OTP02		0	1	1	1	0	0	0	0	70h	
OTP01		0	1	1	1	1	0	0	0	78h	
OTP00	Factory Programmed and Locked	1	0	0	0	0	0	0	0	80h	Not Programmable area

[OTP Read]

Device Information	Bus Status in Reading		Remarks
	Page/Word Add A[14:7]/A[6:0]	Word Data	
OTP0: Factory Programmed OTP	OTP Page ADD: 80h* OTP Word ADD: 00h-3Fh	Factory Programmed Data	Word Address are for A[6:0]
OTPn: User OTP (n=1-16)	OTP Page ADD: 10h-78h* OTP Word ADD: 00h-3Fh	User OTP Data	

When Byte Mode is selected, data of DQ[15:8] and DQ[7:0] in above table will output from DQ[7:0] at A-1=H and A-1=L, respectively.

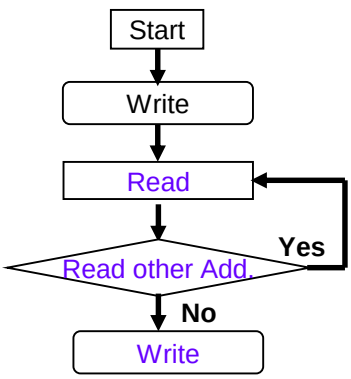
[Program Flow Chart for User OTP Area]



Command	Address	Word Data
User OTP Setup	OTP ADD	XXC1h
User OTP Page Program Setup	OTP Page ADD	XX4Fh
User OTP Page Program Load	OTP Word ADD(0) to OTP Word ADD(63)	PD(0) to PD(63)
User OTP Page Program Confirm 1	OTP Word ADD(64) to OTP Word ADD(79)	0000h
User OTP Page Program Confirm 2	OTP ADD	XXD0h

Check SR[7]	Data
WSM Ready	1
WSM Busy	0

[Read Flow Chart of User OTP Area]



Command	Address	Word Data
User OTP Entry	OTP ADD	XXC1h
Exit User OTP Read	Don't Care	XXFFh

Need 1ms wait time after command input of read of User OTP Area.

Absolute Maximum Ratings

Symbol	Parameter	Condition	Min.	Max.	unit
VCC	VCC Supply Voltage	Referenced to VSS	-0.2	2.5	V
VCCQ	VCCQ Supply Voltage		-0.2	4.0	V
VI1	Input Voltage		-0.5	VCC+0.5	V
Tbs	Storage Temperature w/ Bias		-50	95	℃
Tstg	Storage Temperature w/o Bias		-65	125	℃
Iout	Output Short Circuit Current			100	mA

Operating Ranges

Symbol	Parameter	Min.	Max.	unit
VCC	VCC Supply Voltage	1.7	2.0	V
VCCQ	VCCQ Supply Voltage	1.7	2.0	V
		2.7	3.6	V
Ta	Ambient Operation Temperature	0	70	℃

DC Characteristics(1)

Symbol	Parameter		Condition	Min.	Typ.	Max.	unit
ILI	Input Leakage Current		0V≤ VIN ≤VCCQ			±2	uA
ILO	Output Leakage Current		0V≤ VOUT ≤VCCQ			±2	uA
ICC1	Read Current	Random Read	CEn#=VIL, OE#=VIH, f=5MHz		57	65	mA
		Page Read	CEn#=VIL, OE#=VIH, f=20MHz(Averaged)		14	20	mA
ICCR	Reset Current		RESET#=GND		70	200	uA
ICC2	Standby Current		CE1#=CE2#=RESET# =VCCQ±0.2V		1000	1200	uA
ICC3	Program Current				35	45	mA
ICC4	Erase Current				32	40	mA
VLKO	VCC Lock Voltage			1.0			V

Caution: CEn# (n=1,2) must not be “L”, simultaneously. When CEn#(n=1,2) is “L”, CEm#(m<>n) must be remained “H”.

DC Characteristics(2) [VCCQ=1.7V-2.0V]

Symbol	Parameter	Condition	Min.	Typ.	Max.	unit
VIL	Input Low Voltage		0.0		0.4	V
VIH	Input High Voltage		VCCQ-0.4		VCCQ	V
VOL	Output Low Voltage	VCC=VCCQ=VCCMin, IOL=100uA, IOH=-100uA			0.1	V
VOH	Output High Voltage		VCCQ-0.1			V

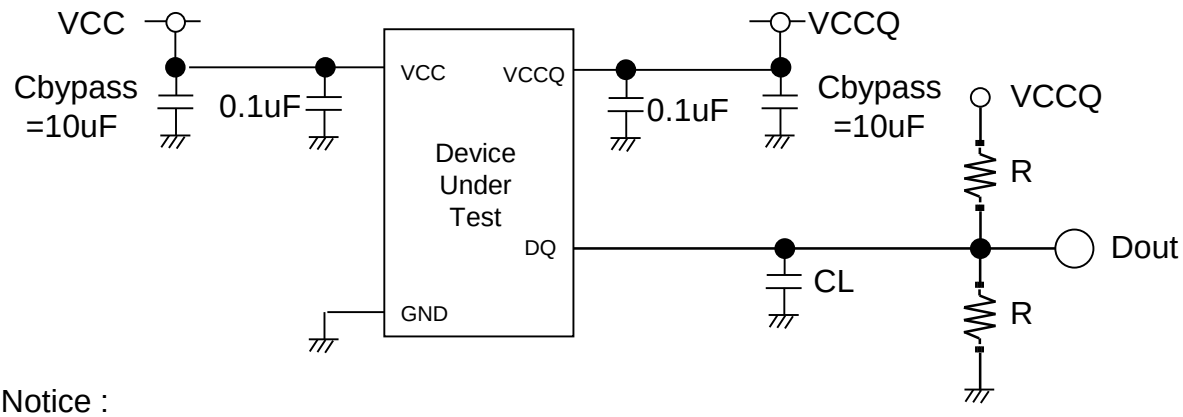
DC Characteristics(3) [VCCQ=2.7V-3.6V]

Symbol	Parameter	Condition	Min.	Typ.	Max.	unit
VIL	Input Low Voltage	VCC≥2.7V	-0.5		0.8	V
VIH	Input High Voltage		0.7VCCQ		VCCQ+0.4	V
VOL	Output Low Voltage	VCC=VCCMin, VCCQ=VCCQMin, IOL=100uA, IOH=-100uA			0.15VCCQ	V
VOH	Output High Voltage		0.85VCCQ			V

Input / Output Capacitance

Symbol	Parameter	Condition	Min.	Max.	unit
CIN	Input Capacitance	VIN=0V	TBD	24	pF
COUT	Output Capacitance	VOUT=0V	TBD	24	pF

[AC Test Conditions]



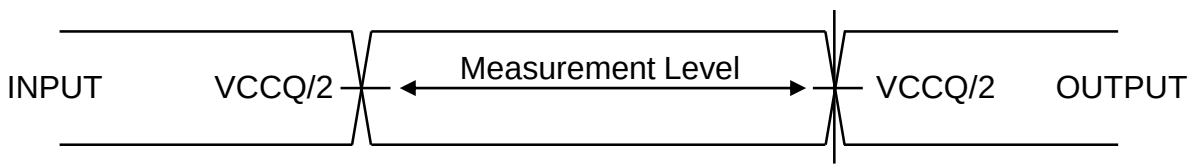
Notice :

1) Simultaneous select of CE1# and CE2# (CE1#=L and CE2#=L) is prohibited.
2) To execute simultaneous programming and erasing of Die0 (CE1#) and Die1 (CE2#), 20uF of Cbypass is recommended.

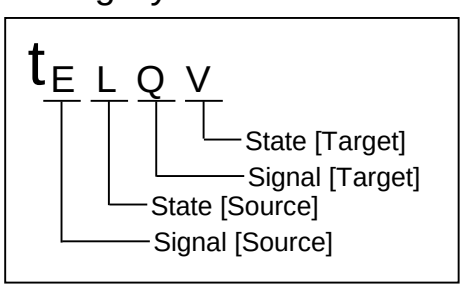
VCC	VCCQ	R(Ohm)
1.8V	1.8V	9K
	3.3V	16.5K

AC Measurement Conditions

Parameter	Min.	Max.	unit
VCC	1.7	2.0	V
VCCQ	1.7	2.0	V
	2.7	3.6	
Output Load Capacitance	30		pF
Input Rise and Fall Time		3	ns
Input pulse Level	0	VCCQ	V
Output timing reference level	VCCQ/2		V
Ambient Temperature	0	70	℃



Timing Symbol Notation



Signal	Symbol	**State**	Symbol
Address	A	High	H
Data -Read	Q	Low	L
Data – Write	D	High-Z	Z
Chip Enable (CEn#)	E	Low-Z	X
Output Enable (OE#)	G	Valid	V
Write Enable (WE#)	W	Invalid	I
Reset (RESET#)	P		

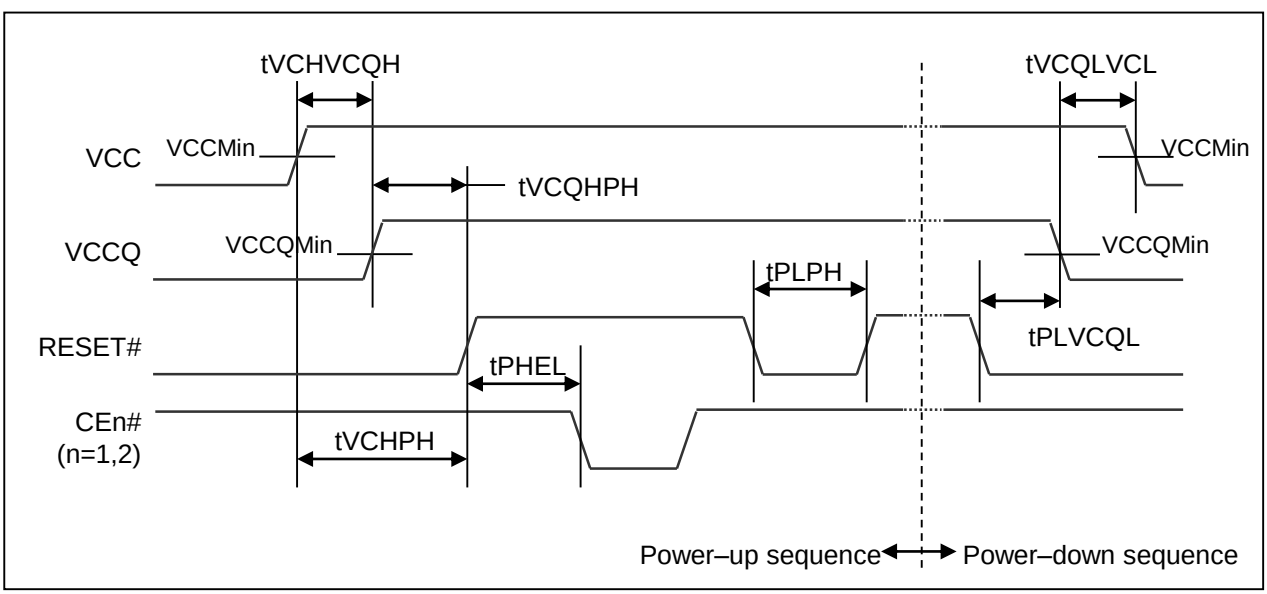
Power up and Reset Timings

Proper Power–up sequence is required to keep the device stable.

1) During power up, RESET# must be kept “L”. RESET# must stay “L” for more than tVCHPH and tVCQHPH, after VCC reaches to VCCmin and VCCQ to VCCQmin.
2) After that, RESET# signal can be set “H”.
3) After RESET# become “H”, CEn# must be kept “H” in the period of tPHEL.

Also, to reset the device effectively, more than the period of tPLPH is required.

Symbol	Parameter	Min.	Max.	unit
tVCHVCQH	VCC High to VCCQ High	0		us
tVCQLVCL	VCCQ Low to VCC Low	0		us
tVCHPH	VCC High to RESET# High	100		us
tVCQHPH	VCCQ High to RESET# High	0		us
tPHEL	RESET# High to CEn# Low	300		us
tPLPH	RESET# Low to High, RESET# Pulse Width	100		us
tPLVCQL	RESET# Low to VCCQ Low	0		us

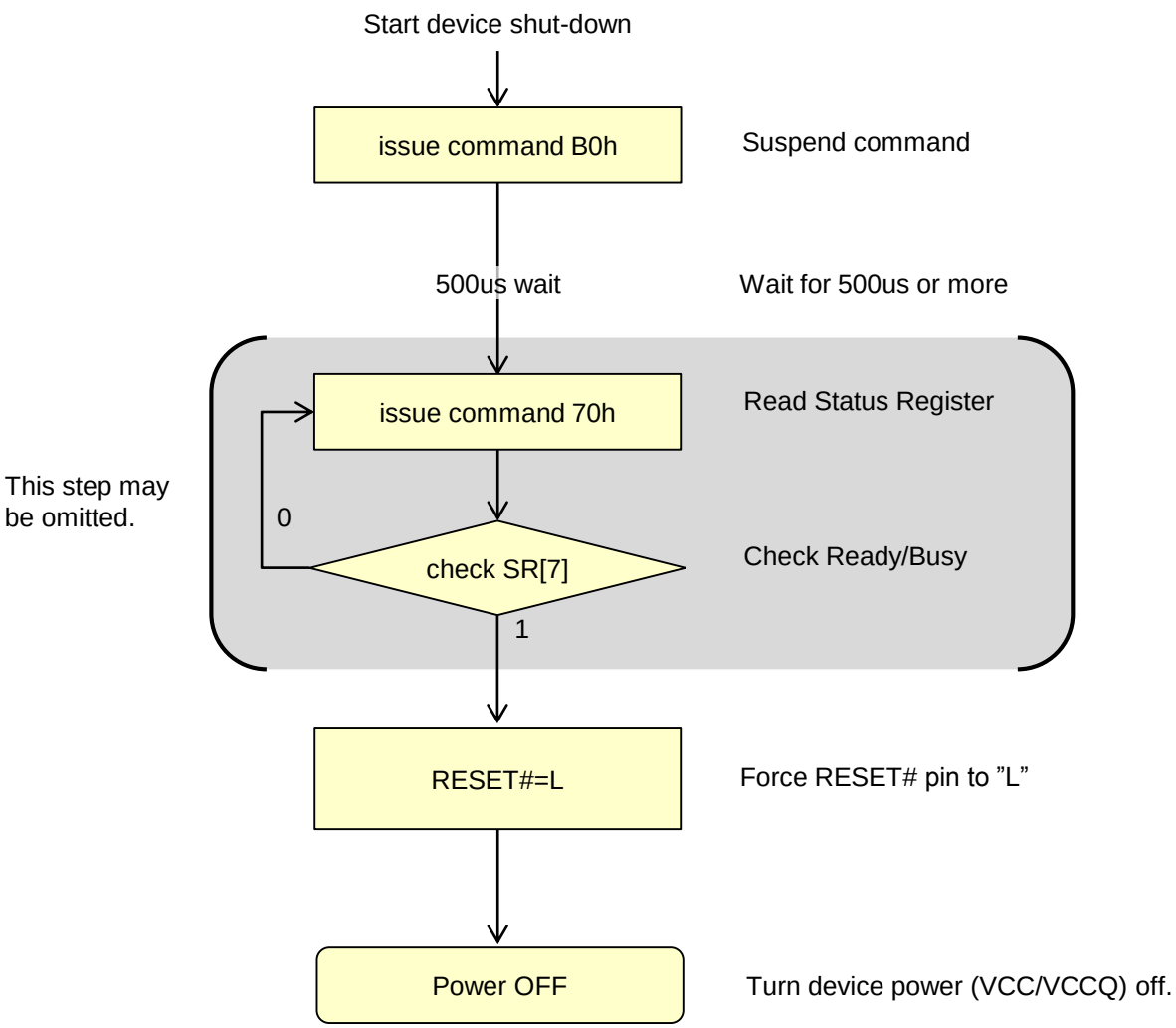


Caution: CEn# (n=1,2) must not be “L”, simultaneously. When CEn#(n=1,2) is “L”, CEm#(m<>n) must be remained “H”.

[Suspend command and shut down sequence]

This device has a suspend command which temporally stops internal operation of program or erase sequence. (please see p.7, p.14, p15)

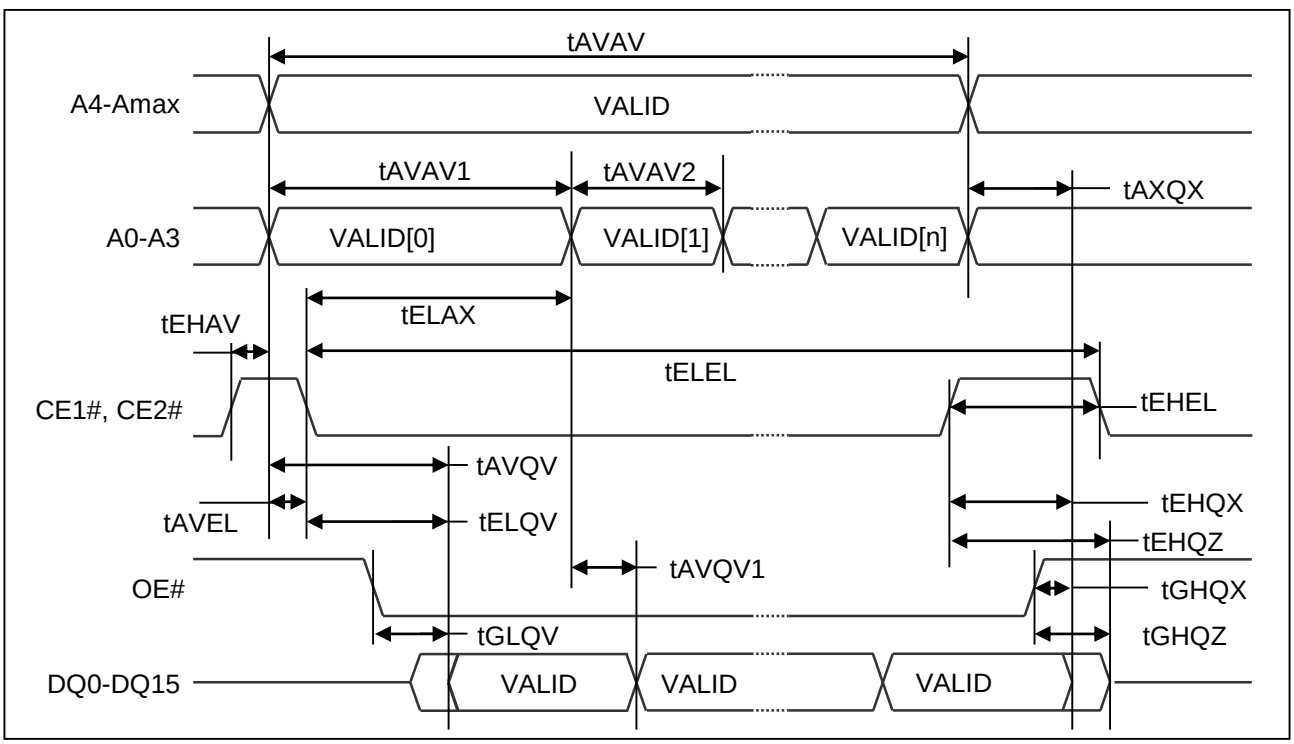
By using steps below, the command is also usable to avoid interferences during device shutting down.



AC Characteristics [Page Read]

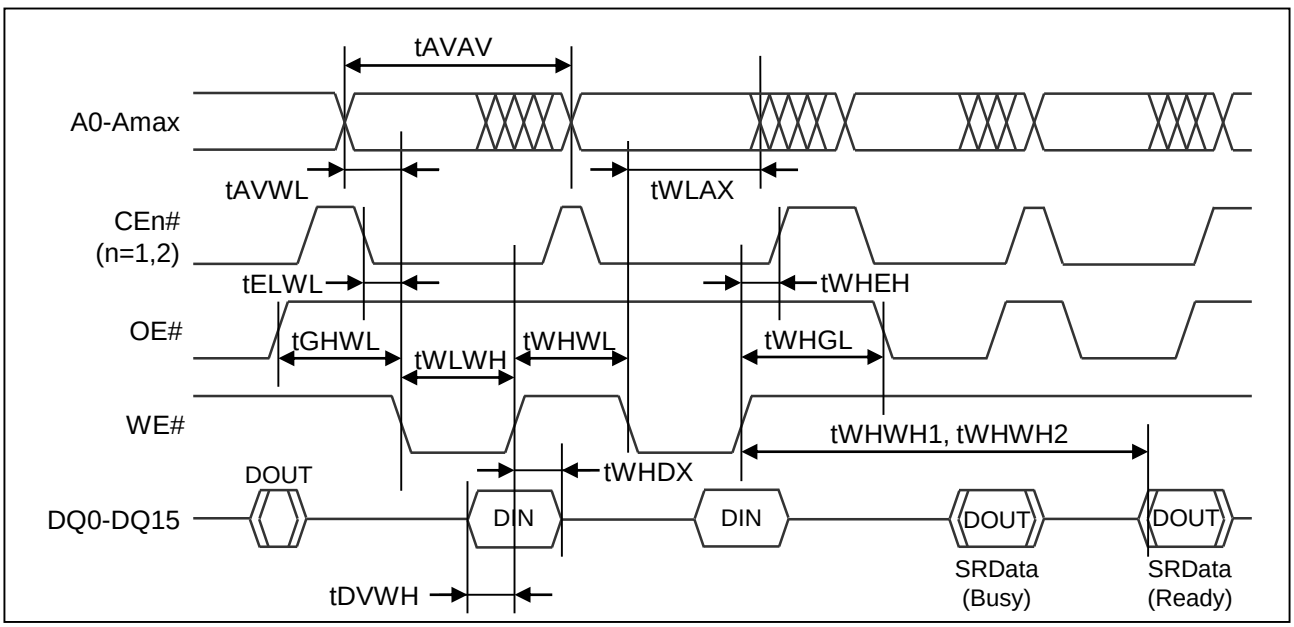
Symbol	Parameter	Min.	Max.	unit
tAVAV1	Address Valid to Next Address Valid for A0~A3 (1st Access), 1st Access Read Cycle Time (A0~A3)	200		ns
tAVAV2	Address Valid to Next Address Valid for A0~A3 (2nd Access), 2nd Access Read Cycle Time (A0~A3)	30		ns
tAVAV	Address Valid to Next Address Valid for A4~Amax, Read Cycle Time (A4~Amax)	670		ns
tAVQV	Address Valid to Output Valid		200	ns
tAVQV1	Address Valid to Output Valid (Page)		30	ns
tELEL	CE# Low to CE# Low	670		ns
tEHEL	CE# High to CE# Low, CE# Pulse Width High	20		ns
tEHAV	CE# High to Address Valid	5		ns
tAVEL	Address Valid to CE# Low, Address Setup Time	0		ns
tELAX	CE# Low to Address Transition	200		ns
tELQV	CE# Low to Output Valid		200	ns
tGLQV	OE# Low to Output Valid		30	ns
tEHQZ	CE# High to Output Hi-Z		20	ns
tGHQZ	OE# High to Output Hi-Z		15	ns
tEHQX tGHQX tAXQX	CE#, OE#, Address Transition to Output Transition	0		ns

Above AC timing specifications are valid in "Page Read Operation"



AC Characteristics [Write (WE# Controlled)]

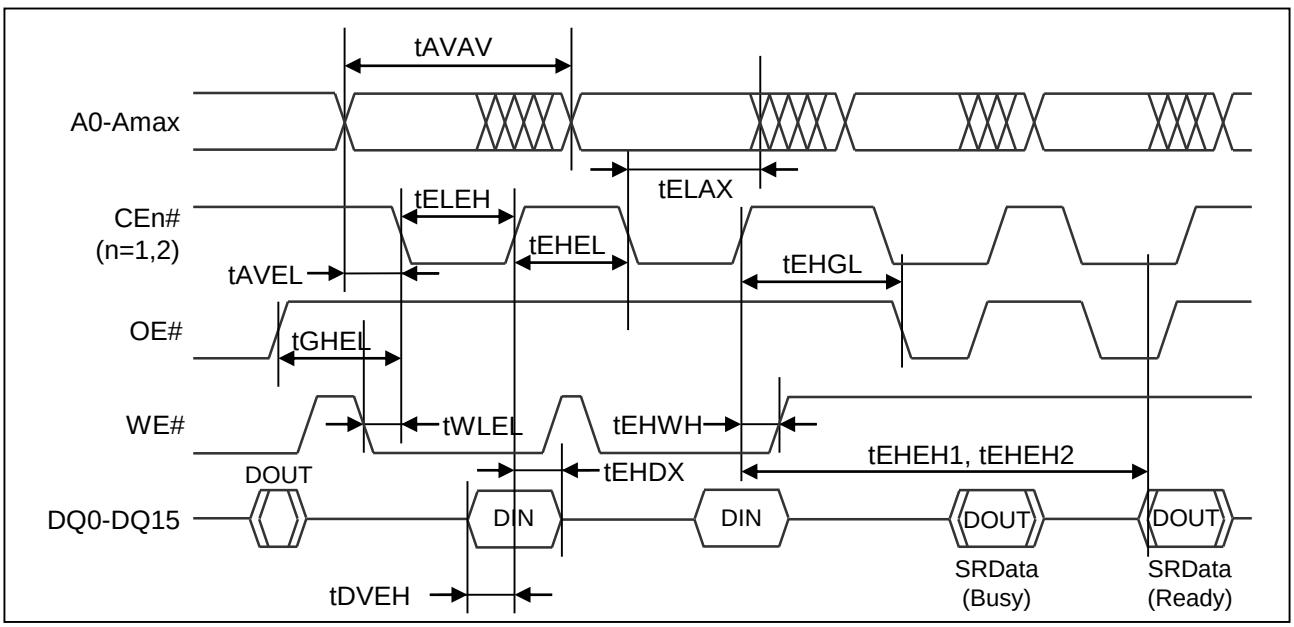
Symbol	Parameter	Min.	Max.	unit
tAVAV	Address Valid to Next Address Valid, Write Cycle time	75		ns
tELWL	CEn# Low to WE# Low, CEn# Setup Time	0		ns
tWLWH	WE# Low to WE# High, Write Pulse Width	35		ns
tDVWH	Input Valid to WE# High, Data Setup Time	30		ns
tWHDX	WE# High to Input Transition, Data Hold Time	0		ns
tWHEH	WE# High to CEn# High, CEn# Hold Time	0		ns
tWHWL	WE# High to WE# Low, Write Pulse Width High	30		ns
tAVWL	Address Valid to WE# Low, Address Setup Time	0		ns
tWLAX	WE# Low to Address Transition, Address Hold Time	45		ns
tGHWL	OE# High to WE# Low, OE# Setup Time	0		ns
tWHGL	WE# High to OE# Low, OE# Hold Time	0		ns



Caution: CEn# (n=1,2) must not be “L”, simultaneously. When CEn#(n=1,2) is “L”, CEm#(m<>n) must be remained “H”.

AC Characteristics [Write (CEn# Controlled)]

Symbol	Parameter	Min.	Max.	unit
tAVAV	Address Valid to Next Address Valid, Write Cycle time	75		ns
tWLEL	WE# Low to CEn# Low, WE# Setup Time	0		ns
tELEH	CEn# Low to CEn# High, CEn# Pulse Width	35		ns
tDVEH	Input Valid to CEn# High, Data Setup Time	30		ns
tEHDX	CEn# High to Input Transition, Data Hold Time	0		ns
tEHWH	CEn# High to WE# High, WE# Hold Time	0		ns
tEHEL	CEn# High to CEn# Low, CEn# Pulse Width High	30		ns
tAVEL	Address Valid to CEn# Low, Address Setup Time	0		ns
tELAX	CEn# Low to Address Transition, Address Hold Time	45		ns
tGHEL	OEn# High to CEn# Low, OE# Setup Time	0		ns
tEHGL	CEn# High to OE# Low, OE# Hold Time	0		ns



Caution: CEn# (n=1,2) must not be “L”, simultaneously. When CEn#(n=1,2) is “L”, CEm#(m<>n) must be remained “H”.

Program and Erase Characteristics

Operation		Parameter	Min.	Typ. *	Max. *	unit
Block Erase	Single	Block Erase Time		100	500	ms
	MultiBank	Multi-Bank Block Erase Time		100	500	ms
	Chip	Chip Erase Time		2		sec
Page Program	Single	Page Program Time		700	3500	us
	MultiBank	Multi-Bank Page Program Time		1000	5000	us
	Chip	Chip Program Time		131		sec
Suspend Latency		Program Suspend Time			250	us
		Erase Suspend Time			500	us

* Conditions Typ.: VCC=1.8V, Ta=RT
Max.: VCC=Operating VCC Range, Ta=Operating Temperature Range,
Program/Erase cycle=10Kcycle

Program and Erase Endurance and Data Retention

Operation	Parameter	Min.	Typ.	Max.	unit
Program and Erase Cycles (Compliant with JEDEC std. JESD47I)	per Block	10K			cycles
Data Retention (Power-Off Data Retention) (Compliant with JEDEC std. JESD47I)					
after 1Kcyc	Data Retention @Ta [55℃]	10			years

[Query Identification String]

(G78FVW002KSQAC)

Offset	Length (Byte)	Query Start Location		Query Data (x16)	Values	Description
		x16	x8			
10h	**3**	**10h**	**20h**	**0051h**	**"Q"**	Query Unique ASCII string "QRY"
		11h	**22h**	**0052h**	**"R"**	
		12h	**24h**	**0059h**	**"Y"**	
13h	**2**	**13h**	**26h**	**000h**	**N/A**	Primary Algorithm Command Set and Control Interface ID code 16-bit ID code defining a specific algorithm
		14h	**28h**	**000h**	**N/A**	
15h	**2**	**15h**	**2Ah**	**0040h**	**offset P=40h**	Address for Primary Algorithm Extended Query Table
		16h	**2Ch**	**0000h**		
17h	**2**	**17h**	**2Eh**	**0000h**	**N/A**	Alternative Algorithm Command Set and Control Interface ID code second specific algorithm supported by the device
		18h	**30h**	**0000h**		
19h	**2**	**19h**	**32h**	**0000h**	**N/A**	Address for Alternative Algorithm Extended Query Table
		1Ah	**34h**	**0000h**		

[Query System Interface Information]

(G78FVW002KSQAC)

Offset	Length (Byte)	Query Start Location		Query Data (x16)	Values	Description
		x16	x8			
1Bh	**1**	**1Bh**	**36h**	**0017h**	**1.7V**	Vcc Logic Supply Minimum Program/Erase or Write voltage. -bits 7-4 : BCD value in volts -bits 3-0 : BCD value in 100 mill volts
1Ch	**1**	**1Ch**	**38h**	**0020h**	**2.0V**	Vcc Logic Supply Maximum Program / Erase or Write voltage. -bits 7-4 : BCD value in volts -bits 3-0 : BCD value in 100 mill volts
1Dh	**1**	**1Dh**	**3Ah**	**0000h**	**N/A**	Vpp[Programming] Supply Minimum Program / Erase voltage. -bits 7-4 : HEX value in volts -bits 3-0 : BCD value in 100 mill volts
1Eh	**1**	**1Eh**	**3Ch**	**0000h**	**N/A**	Vpp[Programming] Supply Maximum Program / Erase voltage. -bits 7-4 : HEX value in volts -bits 3-0 : BCD value in 100 mill volts
1Fh	**1**	**1Fh**	**3Eh**	**0005h**	**32us**	Typical timeout per single word program, 2^n us
20h	**1**	**20h**	**40h**	**0008h**	**128us**	Typical timeout for maximum-size multi-byte program, 2^n us
21h	**1**	**21h**	**42h**	**0009h**	**512ms**	Typical timeout per individual block erase, 2^n ms
22h	**1**	**22h**	**44h**	**0010h**	**64sec**	Typical timeout for full chip erase, 2^n ms
23h	**1**	**23h**	**46h**	**0002h**	**128us**	Maximum timeout for word program, 2^n times typical (offset 1Fh)
24h	**1**	**24h**	**48h**	**0002h**	**1024us**	Maximum timeout for multi-byte program, 2^n times typical (offset 20h)
25h	**1**	**25h**	**4Ah**	**0002h**	**2048ms**	Maximum timeout per individual block erase, 2^n times typical (offset 21h)
26h	**1**	**26h**	**4Ch**	**0002h**	**256sec**	Maximum timeout for chip erase, 2^n times typical (offset 22h)

[Device Geometry Definition]

(G78FVW002KSQAC)

Offset	Length (Byte)	Query Start Location		Query Data (x16)	Values	Description
		x16	x8			
27h	**1**	**27h**	**4Eh**	**001Bh**	**128MB**	Device Size = 2^n in number of bytes (per die)
28h	**2**	**28h**	**50h**	**0002h**	**x8/x16, BYTE#**	Flash Device Interface Code description
		29h	**52h**	**0000h**		
2Ah	**2**	**2Ah**	**54h**	**000Ah**	**1024 bytes**	Maximum number of bytes in multi-byte program = 2^n
		2Bh	**56h**	**0000h**		
2Ch	**1**	**2Ch**	**58h**	**0001h**	**Symmetric**	Number of Erase Block Regions within device bits 7-0 : number of Erase Block Regions
2Dh	**4**	**2Dh**	**5Ah**	**003Fh**	**64Block**	Erase Block Region 1 Information -bits 15-0 = y : y+1 = Number of Erase Blocks of identical size -bits 31-16 = z : Erase Block within this region are (z) times 256bytes in size within the Region 1
		2Eh	**5Ch**	**0000h**		
		2Fh	**5Eh**	**0000h**	**2Mbyte**	
		30h	**60h**	**0020h**		
31h	**4**	**31h**	**62h**	**0000h**	**N/A**	Reserved for future erase block region 2 information
		32h	**64h**	**0000h**		
		33h	**66h**	**0000h**		
		34h	**68h**	**0000h**		
35h	**4**	**35h**	**6Ah**	**0000h**	**N/A**	Reserved for future erase block region 3 information
		36h	**6Ch**	**0000h**		
		37h	**6Eh**	**0000h**		
		38h	**70h**	**0000h**		
39h	**4**	**39h**	**72h**	**0000h**	**N/A**	Reserved for future erase block region 4 information
		3Ah	**74h**	**0000h**		
		3Bh	**76h**	**0000h**		
		3Ch	**78h**	**0000h**		

[Primary Algorithm-Specific Extended Query]

(G78FVW002KSQAC)

Offset	Length (Byte)	Query Start Location		Query Data (x16)	Values	Description
		x16	x8			
40h	**3**	**40h**	**80h**	**0050h**	**"P"**	Query Unique ASCII string "PRI"
		41h	**82h**	**0052h**	**"R"**	
		42h	**84h**	**0049h**	**"I"**	
43h	**1**	**43h**	**86h**	**0031h**	**1**	Major Version number, ASCII
44h	**1**	**44h**	**88h**	**0030h**	**0**	Minor Version number, ASCII
45h	**1**	**45h**	**8Ah**	**0006h**	**Not Required / Rev.1.**	Address sensitive unlock: -bit0 to 1: 00 = Required, 01 = Not Required -bit2 to 7: Silicon Revision number
46h	**1**	**46h**	**8Ch**	**0002h**	**Read & Write**	Erase Suspend: 00 = not supported, 01 = Read only, 02 = read and write
47h	**1**	**47h**	**8Eh**	**0001h**	**1**	Block Protection: 00 = not supported, x = number of blocks per group
48h	**1**	**48h**	**90h**	**0001h**	Supported	Temporary block unprotect: 00 = not supported, 01 = supported
49h	**1**	**49h**	**92h**	**0000h**	**Original**	Block Protect and Unprotect: 00=Original
4Ah	**1**	**4Ah**	**94h**	**0000h**	**N/A**	Simultaneous operation
4Bh	**1**	**4Bh**	**96h**	**0000h**	**N/A**	Burst mode: 00 = not supported, 01 = supported
4Ch	**1**	**4Ch**	**98h**	**0003h**	**16word**	Page mode Read : 00 = Not supported 01 = 8word , 02 = 8word , 03 = 16word
4Dh	**1**	**4Dh**	**9Ah**	**0000h**	**N/A**	Vpp Supply maximum Program/Erase voltage bit7 to 4: HEX value in volts bit3 to 0: BCD value in 100m volts
4Eh	**1**	**4Eh**	**9Ch**	**0000h**	**N/A**	Vpp Supply Optimum Program/Erase voltage bit7 to 4: HEX value in volts bit3 to 0: BCD value in 100m volts
4Fh	**1**	**4Fh**	**9Eh**	**0000h**	**N/A**	Top / Bottom boot block flag 04h = Symmetrically block and H/W protect for lowest block 05h = Symmetrically block and H/W protect for Highest block
50h	**1**	**50h**	**A0h**	**0001h**	Supported	Program Suspend: 00 = not supported, 01 = supported

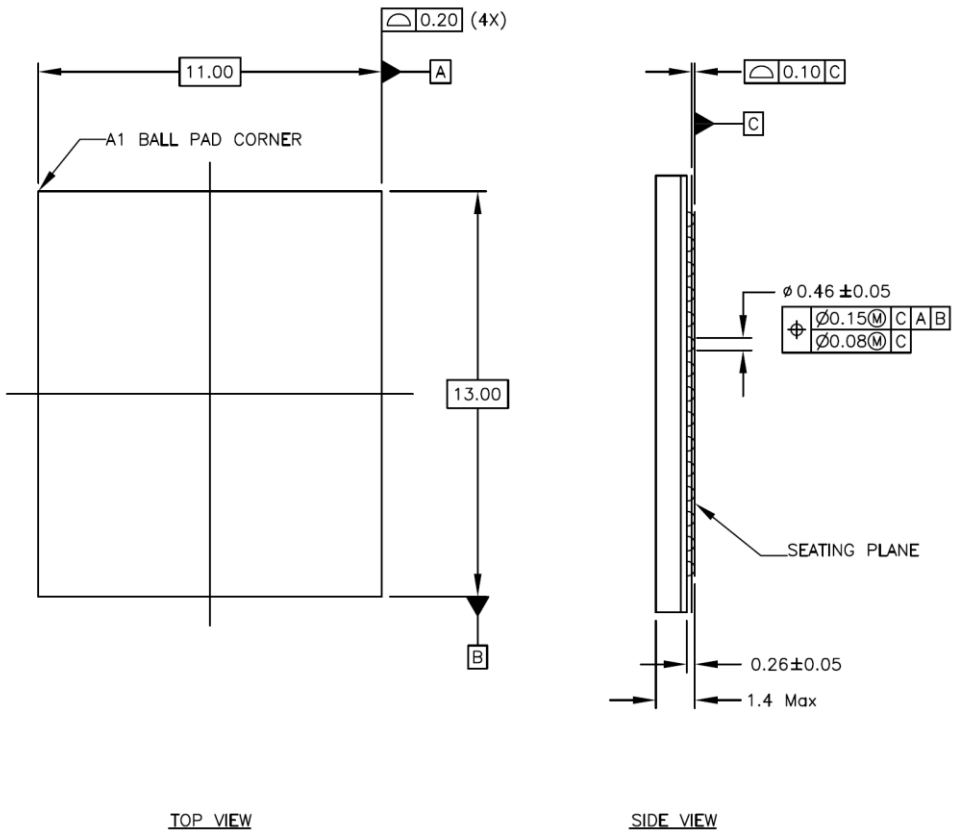
G78FVW002KSQAC

2Gbit NOR type B4-Flash
[128M by 16bit]

Products and specifications indicated to this datasheet are subject to change by GENUSION without notice.

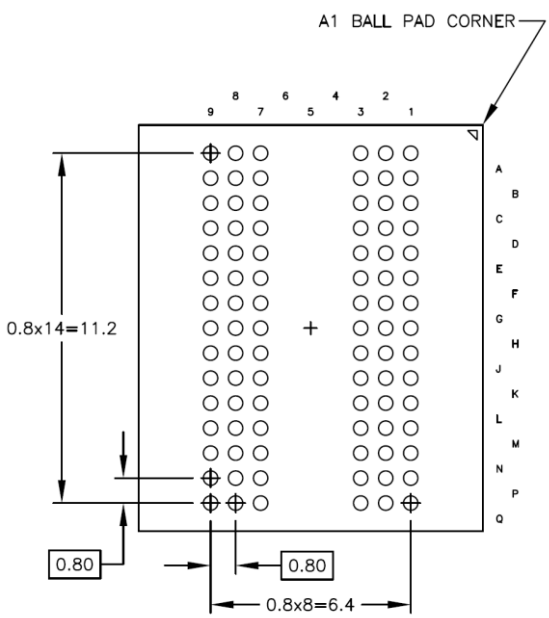
High reliability , high speed and high density

G78FVW002KSQAC Package Outline



TOP VIEW

SIDE VIEW



BOTTOM VIEW
90 SOLDER BALLS