

G78FVW001KSQAE

1Gbit NOR type B4-Flash

[64M by 16bit]

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High reliability , high speed and high density

General Description

The GENUSION G78FVW001KSQ is a NOR flash product of GENUSION's B4-Flash^(*) technology which enables high speed program/erase and high reliability of data retention on high density devices.

The G78FVW001KSQAE is MCP (Multi Chip Package) product which is 2-dies of 512Mbit NOR flash memory packaged in 90-balls FBGA.

*1 : B4-Flash(**B**ack **B**ias assisted **B**and-to-**B**and tunneling induced Hot-Electron injection **F**lash)

Features

●Memory Density

G78FVW001KSQAE : 1G (64Mx16)bit (2CE)

●Word organization

16bit (W: Words)

●Power Supply Voltage

Core (Vcc) : 1.7V~2.0V

I/O (Vccq) : 2.7V~3.6V

●Low Power Consumption

Reset : 0.13mW (Typ.)

Stand by : 1.34mW (Typ.)

Random Read (@5MHz) : 72mW (Typ.)

Page Read : 22mW (Typ.)

Program : 63mW (Typ.)

Erase : 58mW (Typ.)

●Ambient Operation Temperature

-40°C~85°C

●Package:

90balls FBGA (ball pitch: 0.8mm):

11mm x 13mm, height (max) 1.4mm

RoHS compliant

●Page size

(Read): 16W

(Program): 128W

512W (*2)

●Block size

(Erase): 512KW

2MW (*2)

●Access Time

(1st Access):

115ns (max.)

(VCC=1.7V~2.0V)

100ns (max.)

(VCC=1.8V~2.0V)

(2nd Access):

30ns (max.)

●Chip Program Time (*2, *3):

G78FVW001KSQAE:

10sec(typ.)

●Chip Erase Time (*2, *3):

G78FVW001KSQAE:

2sec(typ.)

*2: MBO Multi Bank Operation

*3: MCI Multi Chip Interleave

●Reliability:

Compliant with JEDEC std. JESD47I and Extended Data Retention

Data Retention:

20years@125°C

after 100K P/E cycle

(failure rate of 0.1% per Chip*4)

Program/Erase cycle:

100K cycle/Block

*4: In case JEDEC std. JESD47I,

general failure rate is 1% per Chip.

●Process Technology:

90nm B4-Flash

Target Application

●High density code storage for industrial equipment

●High density code storage for mobile devices

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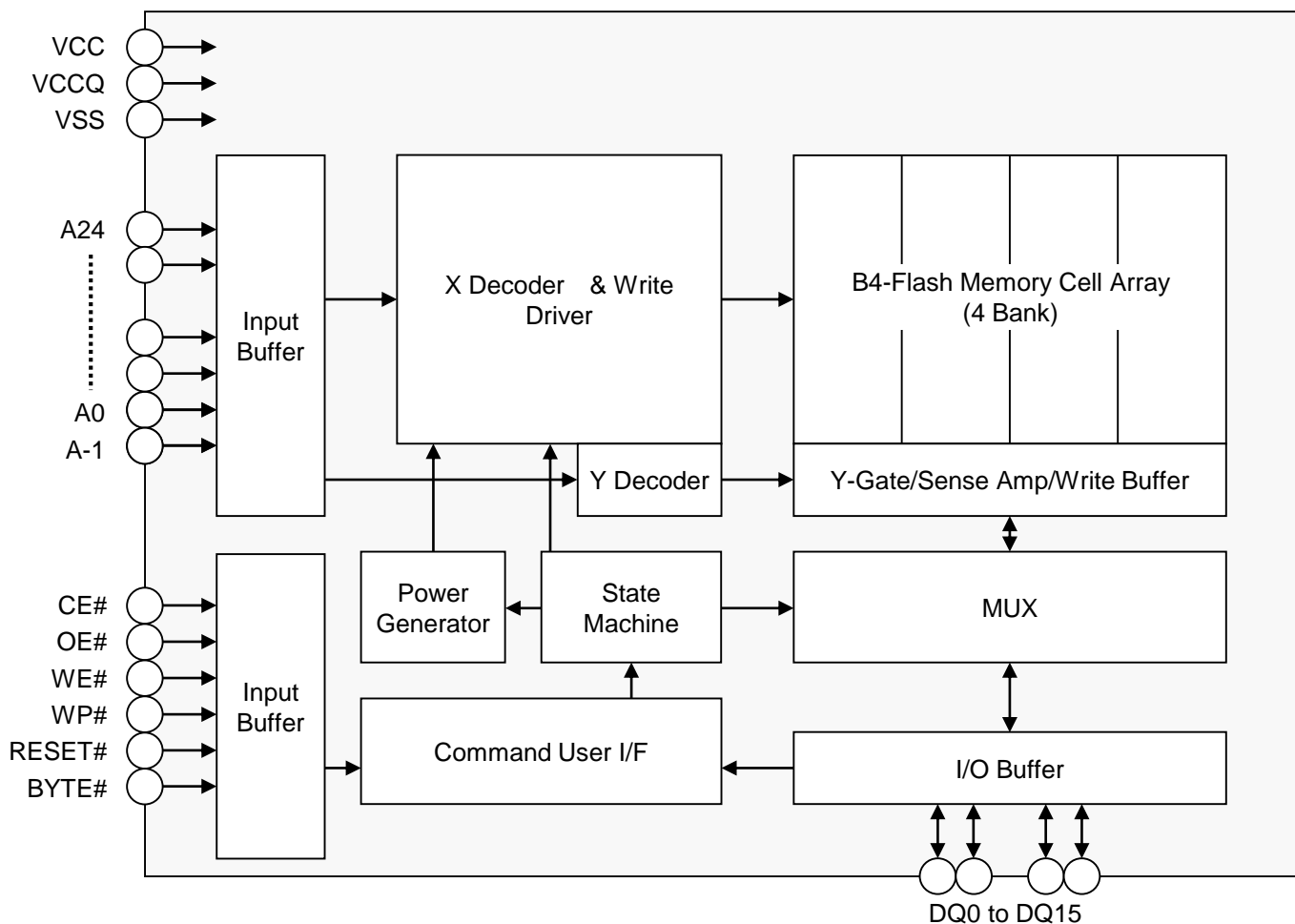
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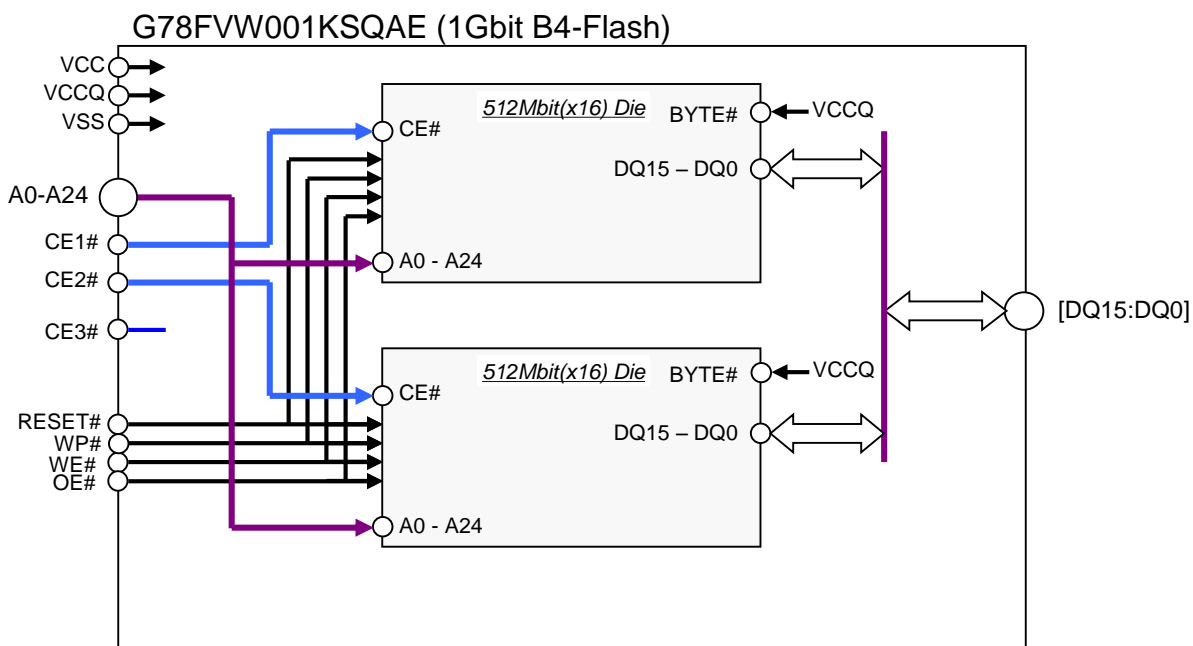
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512Mbit B4-Flash Die Block Diagram



MCP(Multi-Chip Package) Block Diagram



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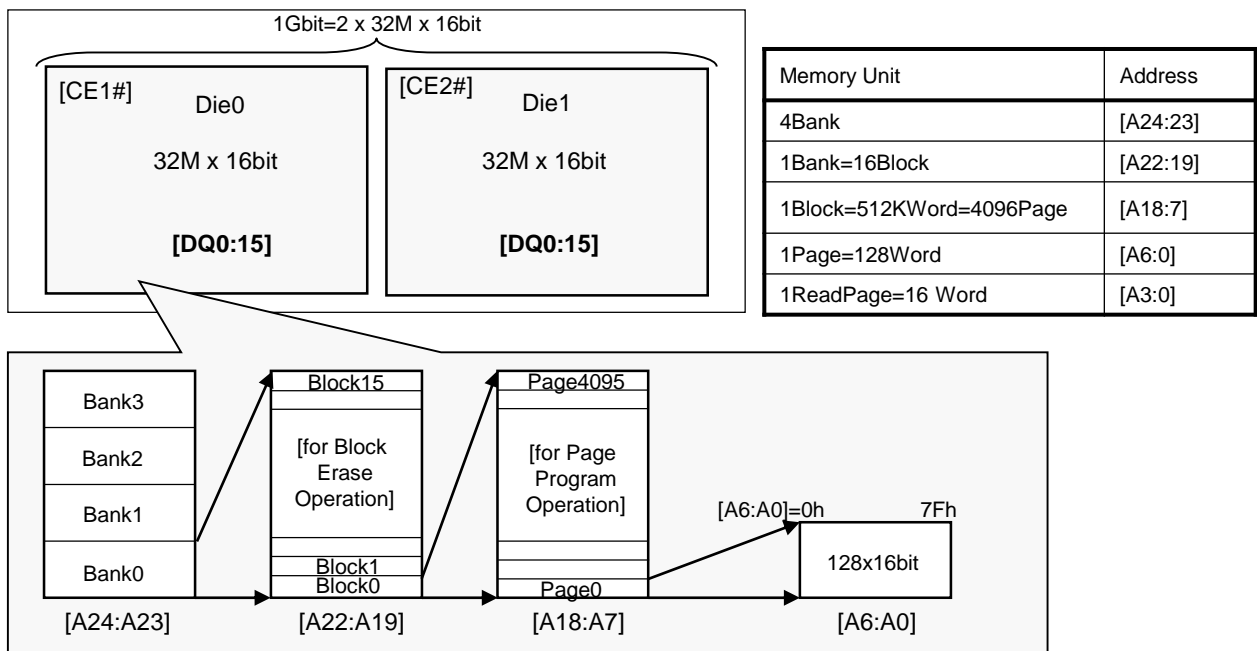
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G78FVW001KSQAE (1Gbit B4-Flash) Memory Map



[Memory Map (CE1#="L" or CE2#="L")]

Bank	BLK	Address	Word
3	63	1FFFFFF hex - 1F80000 hex	512KW
3	62	1F7FFFF hex - 1F00000 hex	512KW
3	61	1EFFFFF hex - 1E80000 hex	512KW
3	60	1E7FFFF hex - 1E00000 hex	512KW
3	59	1DFFFFFF hex - 1D80000 hex	512KW
3	58	1D7FFFF hex - 1D00000 hex	512KW
3	57	1CFFFFFF hex - 1C80000 hex	512KW
3	56	1C7FFFF hex - 1C00000 hex	512KW
3	55	1BFFFFFF hex - 1B80000 hex	512KW
3	54	1B7FFFF hex - 1B00000 hex	512KW
3	53	1AFFFFFF hex - 1A80000 hex	512KW
3	52	1A7FFFF hex - 1A00000 hex	512KW
3	51	19FFFFFF hex - 1980000 hex	512KW
3	50	197FFFF hex - 1900000 hex	512KW
3	49	18FFFFFF hex - 1880000 hex	512KW
3	48	187FFFF hex - 1800000 hex	512KW
2	47	17FFFFFF hex - 1780000 hex	512KW
2	46	177FFFF hex - 1700000 hex	512KW
2	45	16FFFFFF hex - 1680000 hex	512KW
2	44	167FFFF hex - 1600000 hex	512KW
2	43	15FFFFFF hex - 1580000 hex	512KW
2	42	157FFFF hex - 1500000 hex	512KW
2	41	14FFFFFF hex - 1480000 hex	512KW
2	40	147FFFF hex - 1400000 hex	512KW
2	39	13FFFFFF hex - 1380000 hex	512KW
2	38	137FFFF hex - 1300000 hex	512KW
2	37	12FFFFFF hex - 1280000 hex	512KW
2	36	127FFFF hex - 1200000 hex	512KW
2	35	11FFFFFF hex - 1180000 hex	512KW
2	34	117FFFF hex - 1100000 hex	512KW
2	33	10FFFFFF hex - 1080000 hex	512KW
2	32	107FFFF hex - 1000000 hex	512KW

Bank	BLK	Address	Word
1	31	FFFFFFF hex - F80000 hex	512KW
1	30	F7FFFFF hex - F00000 hex	512KW
1	29	EFFFFFFF hex - E80000 hex	512KW
1	28	E7FFFFF hex - E00000 hex	512KW
1	27	DFFFFFFF hex - D80000 hex	512KW
1	26	D7FFFFF hex - D00000 hex	512KW
1	25	CFFFFFFF hex - C80000 hex	512KW
1	24	C7FFFFF hex - C00000 hex	512KW
1	23	BFFFFFFF hex - B80000 hex	512KW
1	22	B7FFFFF hex - B00000 hex	512KW
1	21	AFFFFFFF hex - A80000 hex	512KW
1	20	A7FFFFF hex - A00000 hex	512KW
1	19	9FFFFFFF hex - 980000 hex	512KW
1	18	97FFFFF hex - 900000 hex	512KW
1	17	8FFFFFFF hex - 880000 hex	512KW
1	16	87FFFFF hex - 800000 hex	512KW
0	15	7FFFFFFF hex - 780000 hex	512KW
0	14	77FFFFF hex - 700000 hex	512KW
0	13	6FFFFFFF hex - 680000 hex	512KW
0	12	67FFFFF hex - 600000 hex	512KW
0	11	5FFFFFFF hex - 580000 hex	512KW
0	10	57FFFFF hex - 500000 hex	512KW
0	9	4FFFFFFF hex - 480000 hex	512KW
0	8	47FFFFF hex - 400000 hex	512KW
0	7	3FFFFFFF hex - 380000 hex	512KW
0	6	37FFFFF hex - 300000 hex	512KW
0	5	2FFFFFFF hex - 280000 hex	512KW
0	4	27FFFFF hex - 200000 hex	512KW
0	3	1FFFFFFF hex - 180000 hex	512KW
0	2	17FFFFF hex - 100000 hex	512KW
0	1	FFFFFFF hex - 80000 hex	512KW
0	0	7FFFFF hex - 0 hex	512KW

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G78FVW001KSQAE 90balls FBGA ball Assign(Top View)

	1	2	3	4	5	6	7	8	9				
A	A5	GND	VCCQ	Top View			VCCQ	GND	A13	A			
B	A4	A18	A2				CE1#	A9	A12	B			
C	A6	A0	A3				CE2#	A8	A14	C			
D	A7	A1	A21				WE#	A19	A15	D			
E	A17	DU	WP#				VCC	A10	A22	E			
F	NC_ CE3#	DU	RESET #				A20	A11	A23	F			
G	DU	GNDQ	VCC				GNDQ	NC_ A25	A24	G			
H	DU	DQ11	NC_DQ				DQ4	NC_DQ	A16	H			
J	DQ10	DQ3	NC_DQ				DQ12	NC_DQ	NC_DQ	J			
K	DQ2	NC_DQ	VCCQ				VCCQ	DQ5	NC_DQ	K			
L	DQ0	NC_DQ	NC_DQ				DQ6	DQ13	NC_DQ	L			
M	GND	NC_DQ	DQ9				NC_DQ	DQ7	GND	M			
N	OE#	DQ8	NC_DQ				DQ14	NC_DQ	NC_ A-1	N			
P	VCCQ	NC_DQ	DQ1				NC_DQ	DQ15	VCCQ	P			
R	GNDQ	VCCQ	GNDQ				GNDQ	VCCQ	GNDQ	R			
	1	2	3				4	5	6	7	8	9	

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Pin Name and Function

Symbol	Pin name	Type	Description
A<24:0>	Address	input	Address input.
DQ<15:0>	Data Input / Output	input/output	Input of data/command for writing, output of memory/status data for reading. Or tri-state output when CEn#="H" or OE#="H". Write data will be held by internal latch.
RESET#	Reset	input	By asserting RESET#="L", the internal operation of the flash memory will be terminated. While RESET#="L", input signals (address, data and other controls) are ignored. Also, during power up and down, holding RESET#="L" prevents memory data from unexpected corruption. After changing RESET#="H", the flash memory exits from reset mode and becomes read mode.
CEn# (n=1,2)	Chip Enable	input	When CEn#="L", it enables the device selected; internal circuits and I/Os become active. When CEn#="H", it disables the device and make DQ pins tri-state. Two CEn# can be selected chip in a package.
WE#	Write Enable	input	The address input signals are stored into internal latches at the falling edge of WE#, or at the falling edge of CEn# while keeping WE#="L". The data input signals are stored into internal latches at the rising edge of WE#, or at the rising edge of CEn# while keeping WE#="L".
OE#	Output Enable	input	In read mode, the pin direction of DQs become output, the data of memory or status register will be appeared on DQ pins when OE#="L". DQ pins become high impedance (Hi-Z) when OE#="H".
WP#	Write Protect	input	WP#="L" enables the Locked Down mechanism. When WP#="H", overrides the Locked Down function, enabling Locked Down blocks to be Unlocked with the unlock command. After power up sequence, all blocks start from S/W locked status so that program and erase are prohibited.
VCC	Power Supply	power	Power supply for core (Flash Memory Array and Periphery logics).
VCCQ	I/O Power Supply	power	Power supply for I/O (DQ) pins.
GND	Device Ground	-	All GND pins must be connected to the System Ground.
GNDQ	Device Ground	-	Ground for I/O (DQ) pins. All GNDQ pins must be connected to the System Ground.
NC	No Connect	-	The NC pin is not internally connected to the memory device. The NC pin may be connected to one of the other signal/power lines.
DU	Don't Use	-	The DU pin is internally connected to the memory device. It needs to be isolated from any other signal/power lines.

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[Bus Interface]

Operation	RESET#	CEn#	OE#	WE#	Address	DQ
Reset	"L"	X	X	X	X	Hi-Z
Standby	"H"	"H"	X	X	X	Hi-Z
Output Disable	"H"	"L"	"H"	"H"	X	Hi-Z
Read	"H"	"L"	"L"	"H"	Valid	Dout
Write	"H"	"L"	"H"		Valid	Din
	"H"		"H"	"L"	Valid	Din

Caution: CEn# (n=1,2) must not be "L", simultaneously. When CEn#(n=1,2) is "L", CEm#(m<>n) must be remained "H".

[Read Device Information]

Device Information	Bus Status in Reading		Remarks
	Address	Word Data	
JEDEC Device Manufacturer Code	00h	XX1Ah	GENUSION
Device ID Code	01h	XX01h	Device ID
Block Lock Status	Block ADD+02h	ex: DQ0=Lock Status DQ1=Lock Down Status	Also please see p17-p18
Enhanced Configuration Register	06h	ECR Data	

[Device Manufacturer Code & Device ID Code]

Command	Bus cycle	Address									Word Data	W / R	
		[A24:7]	[A6:0]										
			A6	A5	A4	A3	A2	A1	A0	hex			
JEDEC Device Manufacturer Code	1	BLK	X	X	X	X	X	X	X	X	00h	XX90h	W
	2	X	L	L	H	H	L	L	L	L	18h	XX7Fh	R
	3	X	L	L	H	L	H	L	L	L	14h	XX7Fh	R
	4	X	L	L	H	L	L	L	L	L	10h	XX7Fh	R
	5	X	L	L	L	H	H	L	L	L	0Ch	XX7Fh	R
	6	X	L	L	L	H	L	L	L	L	08h	XX7Fh	R
	7	X	L	L	L	L	H	L	L	L	04h	XX7Fh	R
	8	X	L	L	L	L	L	L	L	L	00h	XX1Ah	R
Device ID Code	1	BLK	X	X	X	X	X	X	X	X	00h	XX90h	W
	2	X	L	L	L	L	L	L	L	H	01h	XX01h	R
	3	X	L	L	L	H	H	H	L	L	0Eh	XX01h	R
	4	X	L	L	L	H	H	H	H	L	0Fh	XX01h	R

(X denotes "Don't Care".)

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[Status Register Definitions]

SR Bit	Name	Definitions	
[15:8]	Reserved	Reserved for Future Use. (being set to "Zero")	
[7]	Ready Status	0	Device in Busy
		1	Device in Ready
[6]	Erase Suspend Status	0	Not in Erase Suspend
		1	In Erase Suspend
[5,4]	Command Sequence Error	00	Program and Erase operation successful
		01	Program Operation Aborted
		10	Erase Operation Aborted
		11	Command Sequence Error
[3]	Reserved	Reserved for Future Use. (being set to "Zero")	
[2]	Program Suspend Status	0	Not in Program Suspend
		1	In Program Suspend
[1]	Block Locked Error	0	Block not Locked
		1	Block Locked / Operation aborted
[0]	Reserved	Reserved for Future Use. (being set to "Zero")	

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[64M by 16bit]

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[Enhanced Configuration Register Definitions]

ECR Bit	Name	Definitions	
[15:3]	Reserved	Reserved for Future Use. (being set to "Zero")	
[2:0]	Output Driver Control	001	1
		010	2
		011	3
		100	4 (default)
		101	5
		110	6
		others	Reserved for Future Use

[Output Driver Control]

ECR [2:0]	Definitions		Output Driver Multiplier	
			VCCQ=3.3V	VCCQ=1.8V
[2:0]	001	1	1/4	1/3
	010	2	1/2	1/2
	011	3	3/4	2/3
	100	4(default)	1	1
	101	5	5/4	3/2
	110	6	3/2	2

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[Command Bus Operation]

Operation Mode		Command Cycle	Command Code		Description
			Address	Data in x16	
Read	Read Array	Setup	Bank ADD	XXFFh	
	Read Status Register	Setup	Bank ADD	XX70h	
	Read Device Information	Setup	Bank ADD	XX90h	
	Read CFI Code	Setup	Bank ADD	XX98h	
Program/Erase	Page Program	Setup1 Setup2 Data Write Confirm	Start ADD Start ADD Word ADD Page ADD	XXE9h Word Count-1 Prog Data XXD0h	Program Start Add Max of Word Count=128 Repeat to 'Word Count' Confirm
	Word Program	Setup Confirm	Word ADD Word ADD	XX41h Prog Data	
	Block Erase	Setup Confirm	Block ADD Block ADD	XX20h XXD0h	
	Program/Erase Suspend	Setup Status Read Read Array	Block ADD Block ADD Block ADD	XXB0h XX70h XXFFh	"Read Status Register" "Read Array"
	Program/Erase Resume	Setup	Block ADD	XXD0h	
Lock Block	Lock Block	Setup Confirm	Block ADD Block ADD	XX60h XX01h	
	Unlock Block	Setup Confirm	Block ADD Block ADD	XX60h XXD0h	
	Lock Down Block	Setup Confirm	Block ADD Block ADD	XX60h XX2Fh	
Register	Clear Status Register	Setup	Bank ADD	XX50h	
	Program Enhanced Configuration Register	Setup Confirm	Reg Data Reg Data	XX60h XX04h	
	Page Program User OTP	Setup1 Setup2 Data Write Confirm1 Confirm2	OTP ADD OTP ADD OTP ADD OTP ADD OTP ADD	XXC1h XX4Fh OTP Data 0000h XXD0h	OTP Entry Setup Program Data Confirm (16cycles) Confirm
	Read User OTP	Setup Exit	OTP ADD Don't Care	XXC1h XXFFh	OTP Entry OTP Exit (Normal Read)

Undefined commands must not be inputted.

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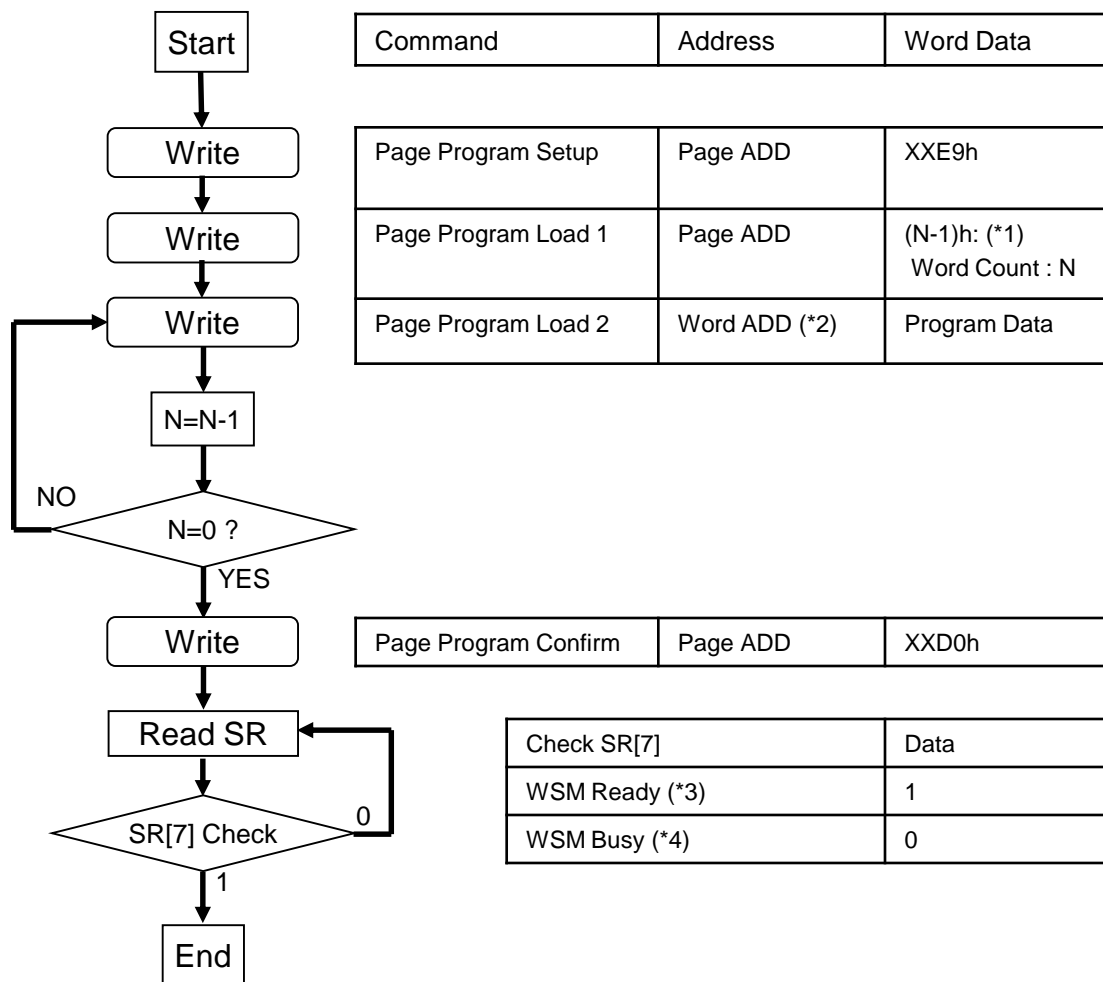
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(1)Page Program Flowchart



Before starting Program operation, status register must be cleared and the block to be programmed must be confirmed as "Unlocked Block" by using Block Lock Status Check (p17-p18). Once a "Page Program" is executed at an address of A[24:4], additional "Program" is prohibited in the same A[24:4] address range unless otherwise erased. During SR[7]=0 (Busy) situation, the only allowed commands are Read Status Register and Program Suspend. After programming has completed(SR[7]=1), any valid command can be issued. To start read array just after programming, Read Array command must be issued.

(*1):Word Count (N) must be multiple of 16, so that, program unit must be n x 16words (n=0 to 7), otherwise Program operation will be aborted as "sequence error". Each 16words must be in address X0h to XFh (X=0 to 7) in A[6:0]. Maximum Word Count (N) is 128 in Word mode and Byte mode, Max of (N-1) = 7Fh.

(*2):Word Address in the page is to be input in A[6:0]. Program address must be in same page address.

(*3):To avoid any interferences, please power off while WSM ready.

(*4):In a situation to shut down while SR[7]=0 (Busy), please follow the sequence shown in p.25.

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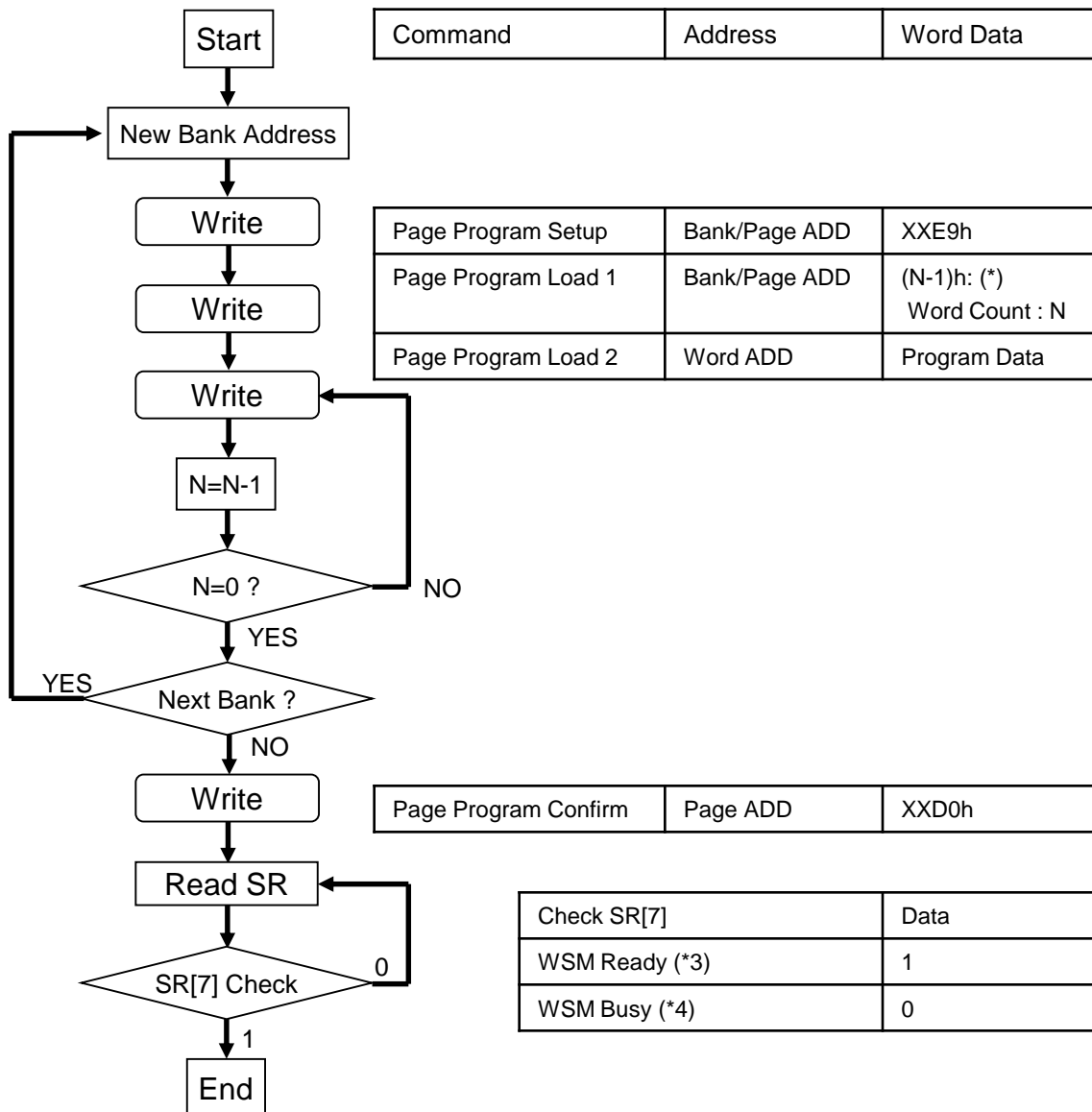
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(2)Multi-Bank Page Program Flowchart



Before starting Program operation, status register must be cleared and the block to be programmed must be confirmed as "Unlocked Block" by using Block Lock Status Check (p17-p18). Once a "Page Program" is executed at an address of A[24:4], additional "Program" is prohibited in the same A[24:4] address range unless otherwise erased. During SR[7]=0 (Busy) situation, the only allowed commands are Read Status Register and Program Suspend. After programming has completed(SR[7]=1), any valid command can be issued. To start read array just after programming, Read Array command must be issued.

- (*1):Word Count (N) must be multiple of 16, so that, program unit must be n x 16words (n=0 to 7), otherwise Program operation will be aborted as "sequence error". Each 16words must be in address X0h to XFh (X=0 to 7) in A[6:0]. Maximum Word Count (N) is 128 in Word mode and Byte mode, Max of (N-1) = 7Fh.
- (*2):Word Address in the page is to be input in A[6:0]. Program address must be in same page address.
- (*3):To avoid any interferences, please power off while WSM ready.
- (*4):In a situation to shut down while SR[7]=0 (Busy), please follow the sequence shown in p.25.

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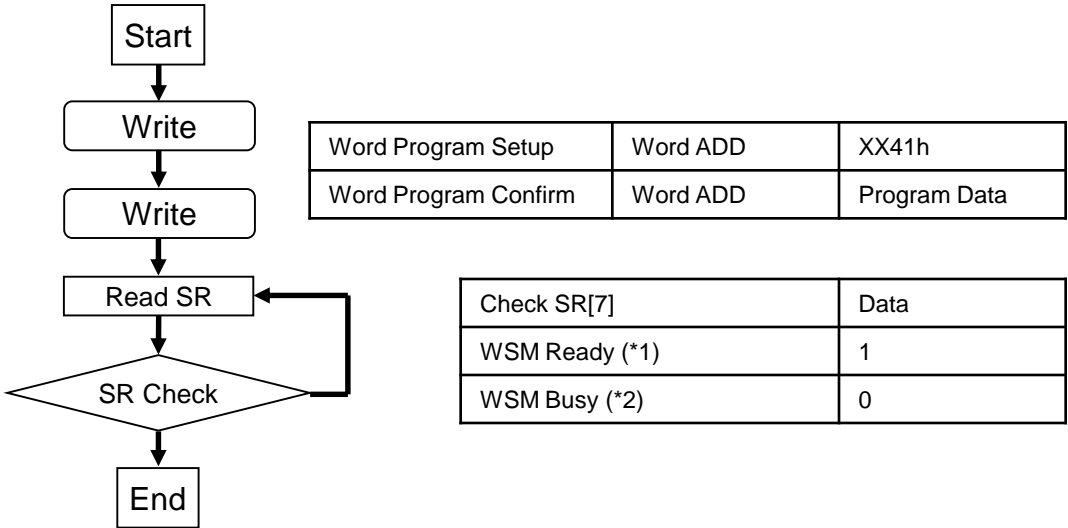
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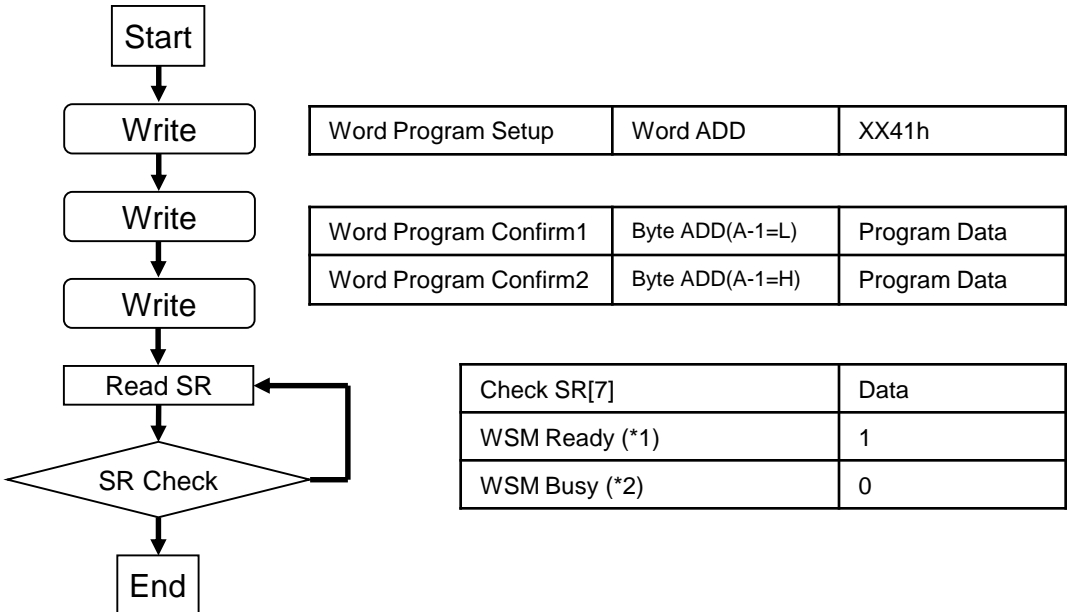
(3)Word Program Flowchart

[in Word Mode (BYTE#="H")]



Word Program operation must be executed at an address where all data of 16 word group, A[3:0] 0h-Fh, are Blank state. Therefore, once a "Word Program" is executed at an address of A[24:4], consecutive "Word Program" is prohibited in the same A[24:4] address range unless otherwise erased. During SR[7]=0 (Busy) situation, the only allowed commands are Read Status Resister and Program Suspend. After programming has completed(SR[7]=1), any valid command can be issued.

[in Byte Mode (BYTE#="L")]



"Single Byte Program" is not supported. Word Program operation must be executed at an address where all data of 16 word group, A[3:0] 0h-Fh, are Blank state. Therefore, once a "Word Program" is executed at an address of A[24:4], consecutive "Word Program" is prohibited in the same A[24:4] address range unless otherwise erased. During SR[7]=0 (Busy) situation, the only allowed commands are Read Status Resister and Program Suspend. After programming has completed(SR[7]=1), any valid command can be issued.

(*1):To avoid any interferences, please power off while WSM ready.
 (*2):In a situation to shut down while SR[7]=0 (Busy), please follow the sequence shown in p.25.

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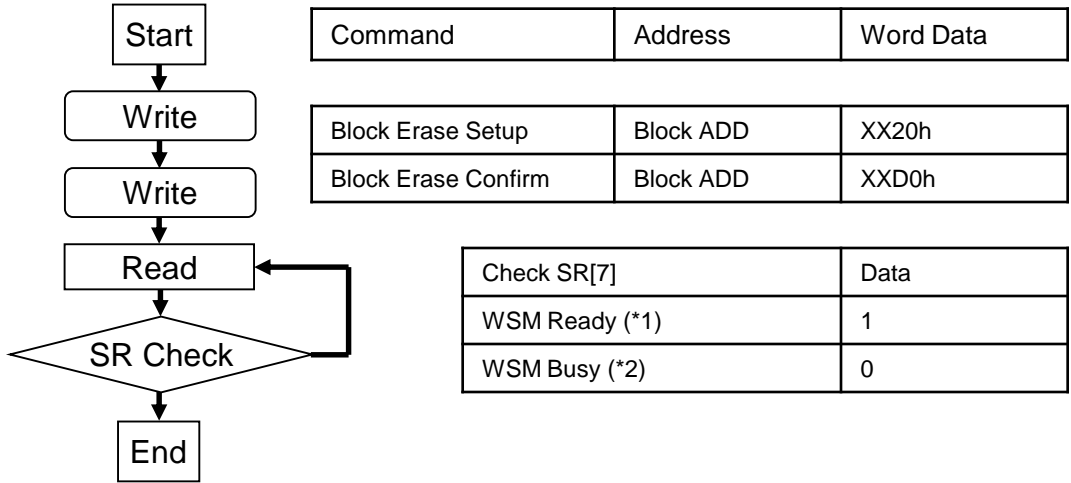
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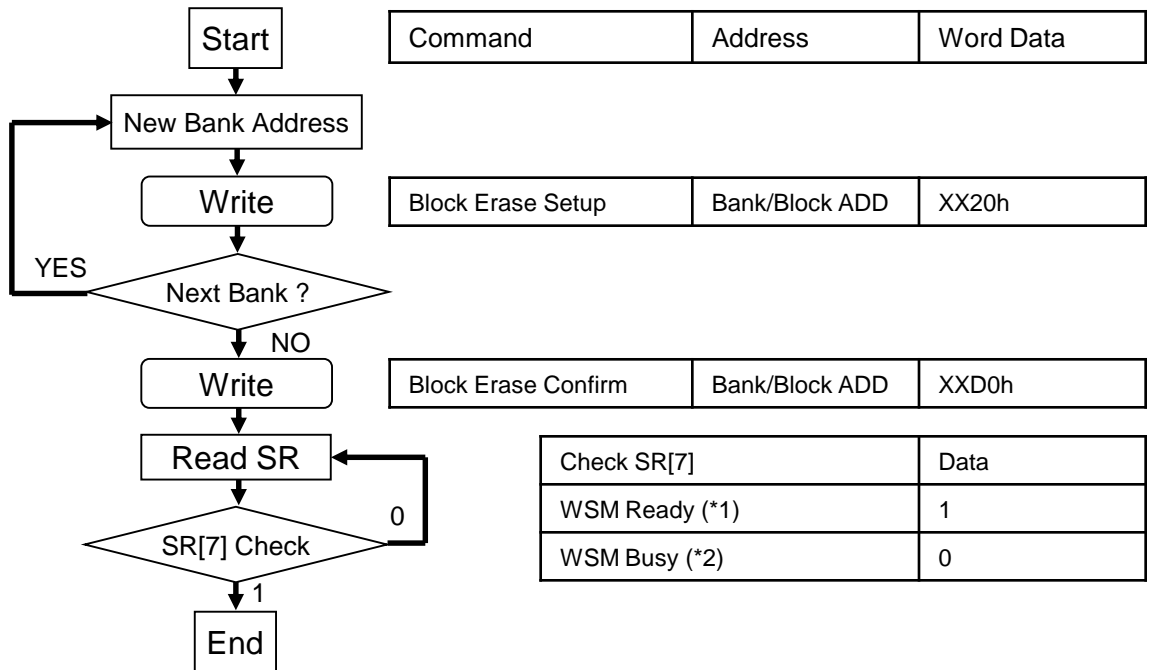
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(4)Block Erase Flowchart



Before start Erase operation, status register must be cleared and the block to be erased must be confirmed as "Unlock Block" using Block Lock Status Check. During SR[7]=0 (Busy) situation, the only allowed commands are Read Status Resister and Erase Suspend. After erasing has completed(SR[7]=1), any valid command can be issued. To start read array just after erasing, Read Array command must be issued.

(5)Multi-Bank Block Erase Flowchart



Before start Erase operation, status register must be cleared and the block to be erased must be confirmed as "Unlock Block" using Block Lock Status Check. During SR[7]=0 (Busy) situation, the only allowed commands are Read Status Resister and Erase Suspend. After erasing has completed(SR[7]=1), any valid command can be issued. To start read array just after erasing, Read Array command must be issued.

(*1):To avoid any interferences, please power off while WSM ready.

(*2):In a situation to shut down while SR[7]=0 (Busy), please follow the sequence shown in p.25.

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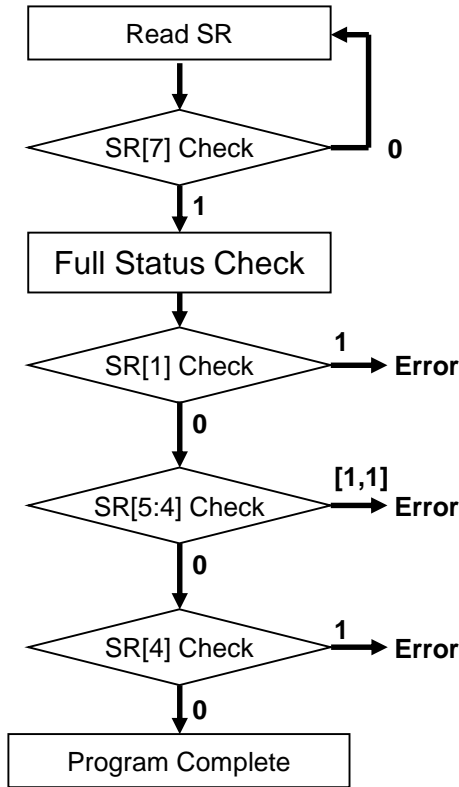
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(6) Program Status Check Flowchart



Check SR[7]	Data
WSM Ready (*1)	1
WSM Busy (*2)	0

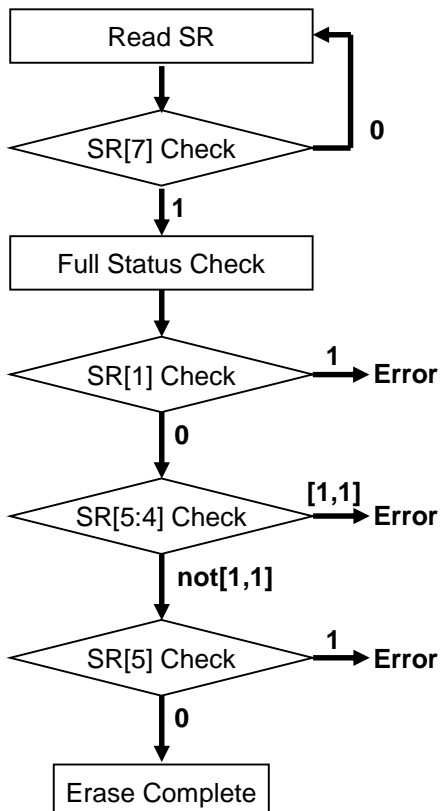
Check SR[1]	Data
Block Locked	1
Block Unlocked	0

Check SR[5:4]	Data
Sequence Error	[1,1]
Sequence OK	Not[1,1]

Check SR[4]	Data
Program Error	1
Program OK	0

If an error is detected, the Status Register should be cleared before continuous operations. Only the Clear Status Register Command clears the Status Register error bits.

(7) Erase Status Check Flowchart



Check SR[7]	Data
WSM Ready (*1)	1
WSM Busy (*2)	0

Check SR[1]	Data
Block Locked	1
Block Unlocked	0

Check SR[5:4]	Data
Sequence Error	[1,1]
Sequence OK	Not[1,1]

Check SR[5]	Data
Erase Error	1
Erase OK	0

(*1): To avoid any interferences, please "power off" or "Reset" while WSM ready.

(*2): In a situation to shut down while SR[7]=0 (Busy), please follow the sequence shown in p.25.

G78FVW001KSQAE

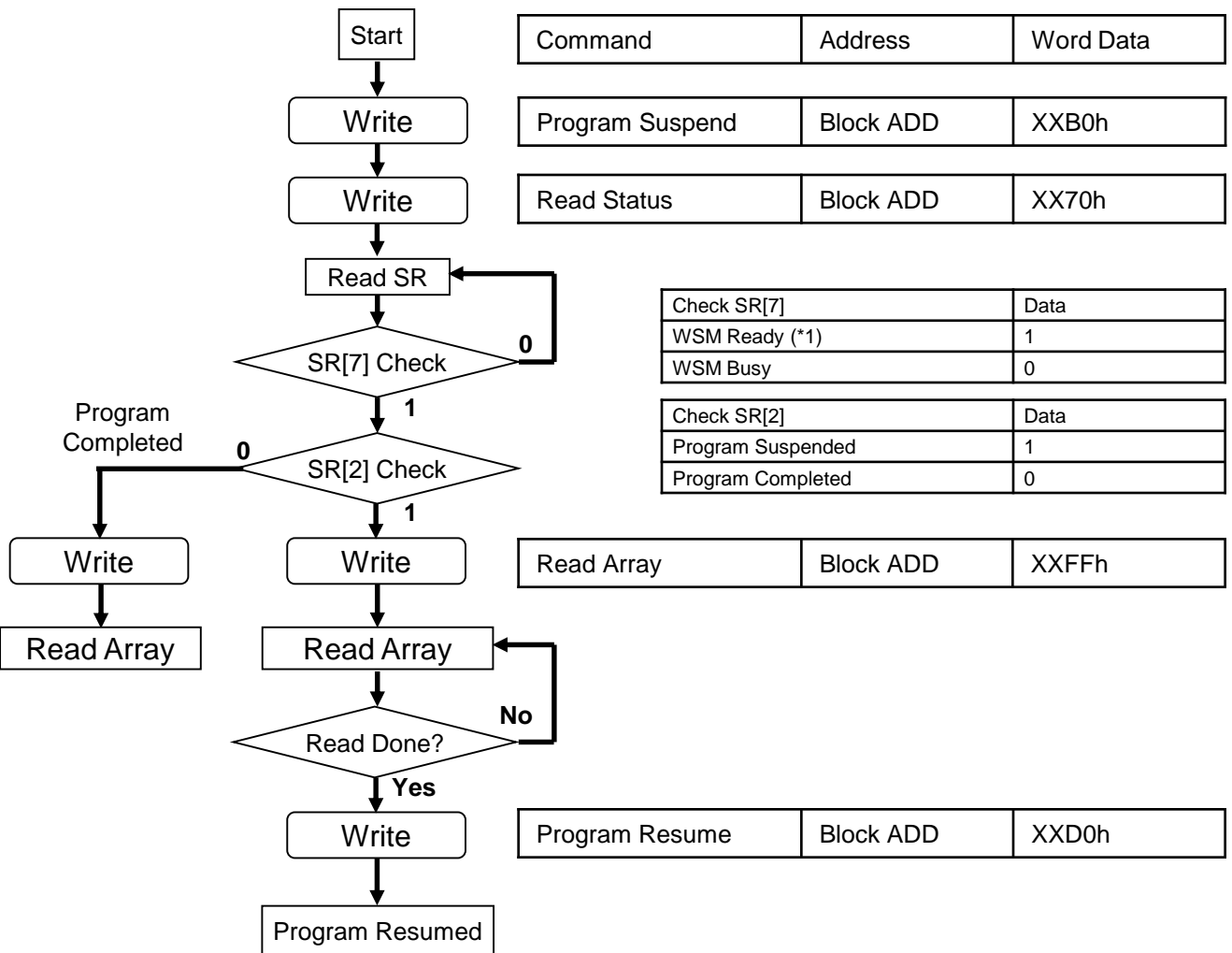
1Gbit NOR type B4-Flash

[64M by 16bit]

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(8)Program Suspend, Read Array and Resume Flowchart



Before starting Program operation, status register must be cleared and the block to be programmed must be confirmed as "Unlocked Block" by using Block Lock Status Check (p17-p18). During SR[7]=0 (Busy) situation, the only allowed commands are Read Status Register and Program Suspend. After programming has completed(SR[7]=1), any valid command can be issued. To start read array just after programming, Read Array command must be issued. In case of SR[7]=0 after waiting the latency period of Suspend command, please RESET referring the procedure on P.24.

(*1):

- To avoid any interferences, please power off while WSM ready.
- After suspended, device can be powered off in safety.

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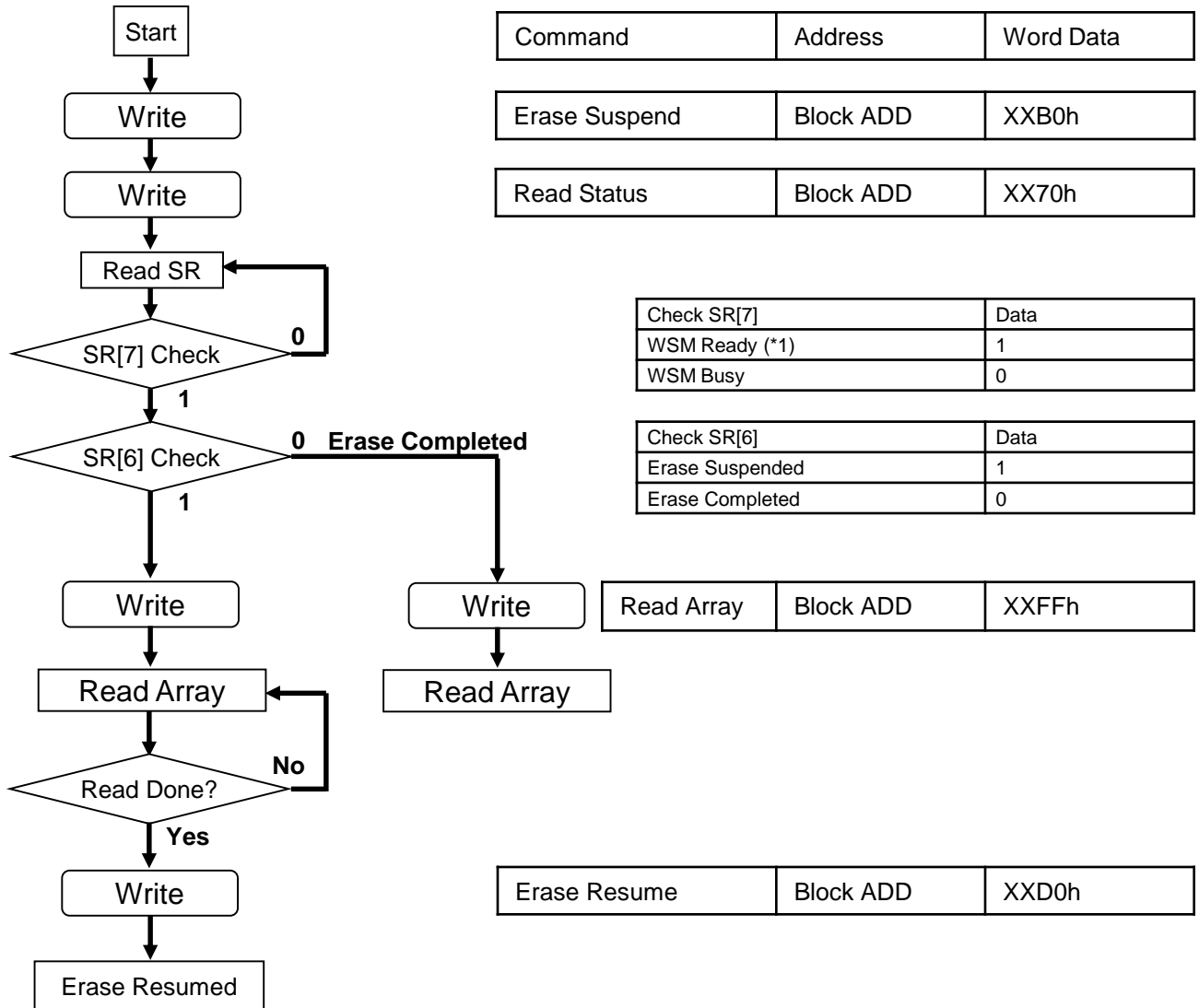
1Gbit NOR type B4-Flash

[64M by 16bit]

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(9)Erase Suspend, Read Array and Resume Flowchart



Before starting Erase operation, status register must be cleared and the block to be erased must be confirmed as "Unlocked Block" by using Block Lock Status Check (p17-p18).
 During SR[7]=0 (Busy) situation, the only allowed commands are Read Status Register and Erase Suspend. After programming has completed(SR[7]=1), any valid command can be issued.
 To start read array just after programming, Read Array command must be issued.
 In case of SR[7]=0 after waiting the latency period of Suspend command, please RESET referring the procedure on P.24.

(*1):

- To avoid any interferences, please power off while WSM ready.
- After suspended, device can be powered off in safety.

G78FVW001KSQAE

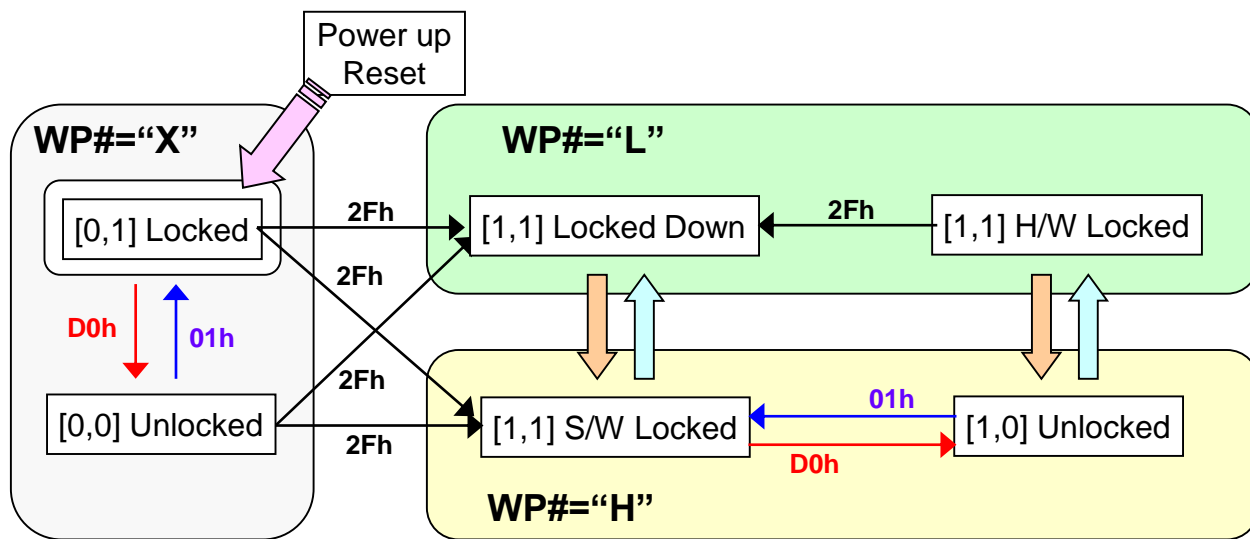
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[Block Lock Status]



[x,x] indicates [DQ1,DQ0]

DQ0: Lock State

"1"-Lock State

"0"-Unlock State

DQ1: Lock Down State

"1"-Lock Down Select

"0"-Lock Down Unselect

mode	WP#	Lock Status Bit [DQ1,DQ0]	Locked BLK	Remarks
Lock Down	"L"	[1,1]	All Block	
H/W Locked				
S/W Locked	"H"	[1,1]	Lock Down Block	
Locked		[0,1]	Lock Block	All Block is locked after Power-Up and Reset.
Unlocked		[1,0]	Unlock Block	

Command	Setup		Confirm	
	Address	Word Data	Address	Word Data
Lock Block	Block Add	XX60h	Block Add	XX01h
Unlock Block	Block Add	XX60h	Block Add	XXD0h
Lock Down Block	Block Add	XX60h	Block Add	XX2Fh

G78FVW001KSQAE

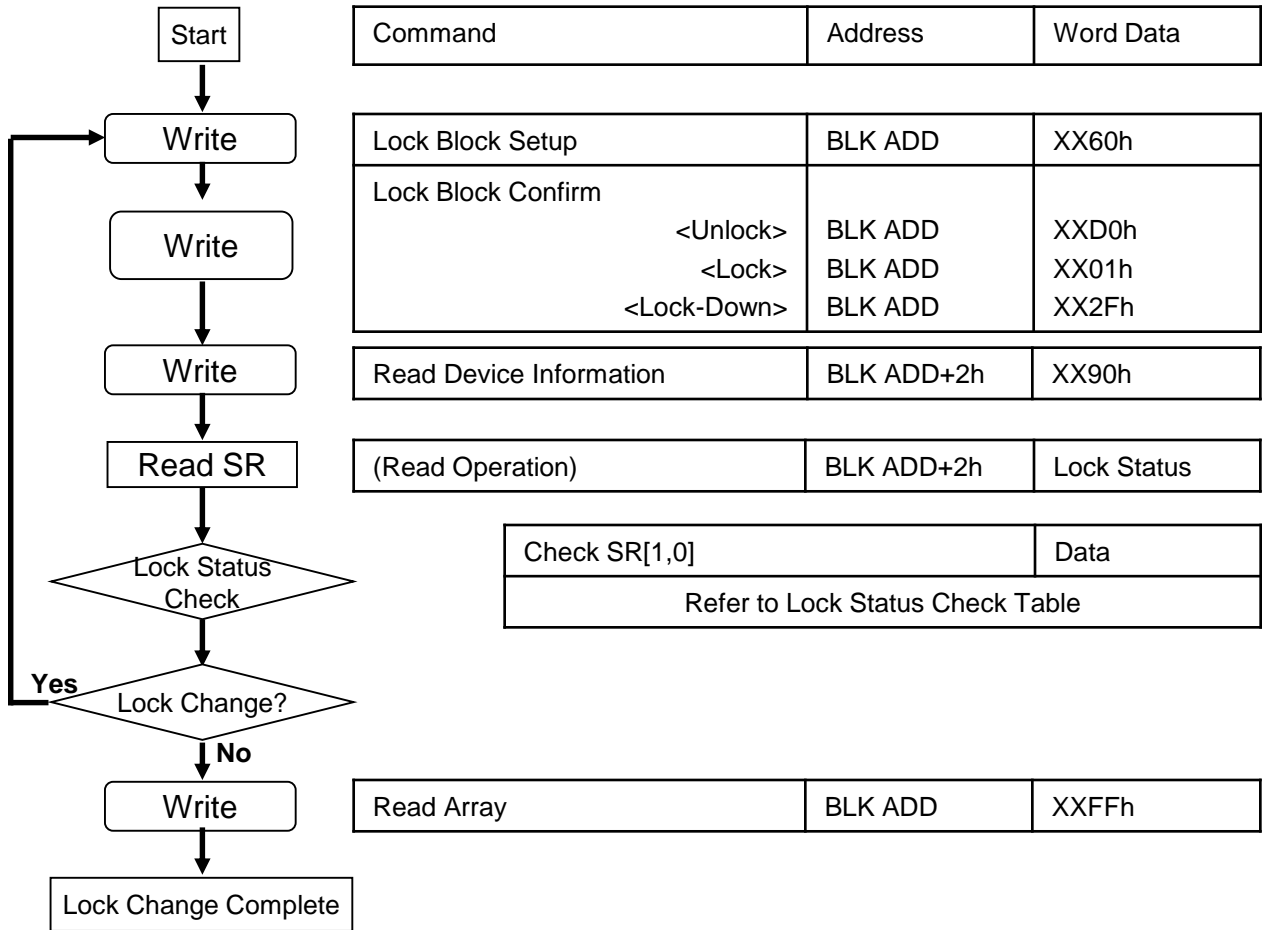
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[Block Lock/Unlock Flow Chart]



Block Lock, Lock Down and Unlock command must not be issued during "Busy" (SR[7]=0), Program suspend and Erase suspend (SR[6]or[2]=1).

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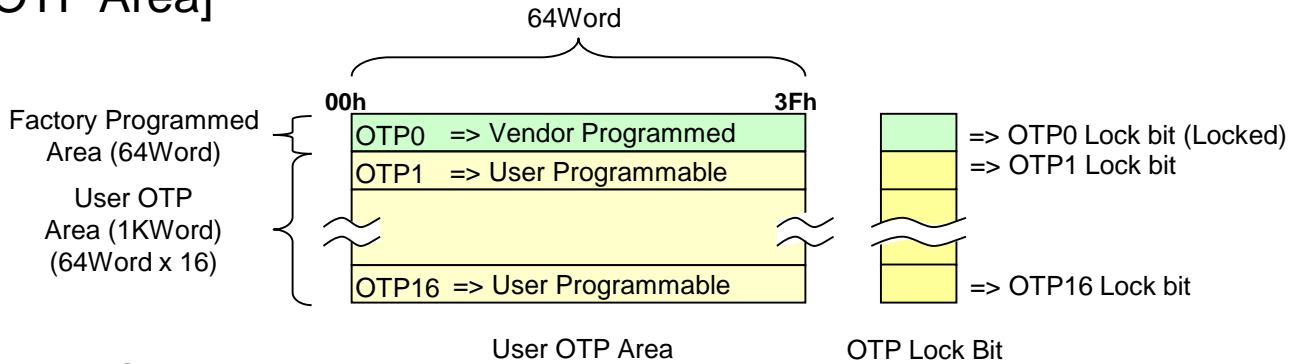
1Gbit NOR type B4-Flash

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[OTP Area]



[User OTP]

OTP Area		OTP Area Address in x16 mode									
OTP #	Function	Page Address A14-A7									Word Address
		A14	A13	A12	A11	A10	A9	A8	A7	Hex	A6-A0
OTP16	User Programmable OTP	0	0	0	0	0	0	0	0	00h	Area size : 64Word 00h-3Fh in A6 – A0 as Word Address.(A6=L) In User OTP area, A15-A24 will be ignored.
OTP15		0	0	0	0	1	0	0	0	08h	
OTP14		0	0	0	1	0	0	0	0	10h	
OTP13		0	0	0	1	1	0	0	0	18h	
OTP12		0	0	1	0	0	0	0	0	20h	
OTP11		0	0	1	0	1	0	0	0	28h	
OTP10		0	0	1	1	0	0	0	0	30h	
OTP09		0	0	1	1	1	0	0	0	38h	
OTP08		0	1	0	0	0	0	0	0	40h	
OTP07		0	1	0	0	1	0	0	0	48h	
OTP06		0	1	0	1	0	0	0	0	50h	
OTP05		0	1	0	1	1	0	0	0	58h	
OTP04		0	1	1	0	0	0	0	0	60h	
OTP03		0	1	1	0	1	0	0	0	68h	
OTP02		0	1	1	1	0	0	0	0	70h	
OTP01		0	1	1	1	1	0	0	0	78h	
OTP00	Factory Programmed and Locked	1	0	0	0	0	0	0	0	80h	Not Programmable area

[OTP Read]

Device Information	Bus Status in Reading		Remarks
	Page/Word Add A[14:7]/A[6:0]	Word Data	
OTP0: Factory Programmed OTP	OTP Page ADD: 80h* OTP Word ADD: 00h-3Fh	Factory Programmed Data	Word Address are for A[6:0]
OTPN: User OTP (n=1-16)	OTP Page ADD: 00h-78h* OTP Word ADD: 00h-3Fh	User OTP Data	

When Byte Mode is selected, data of DQ[15:8] and DQ[7:0] in above table will output from DQ[7:0] at A-1=H and A-1=L, respectively.

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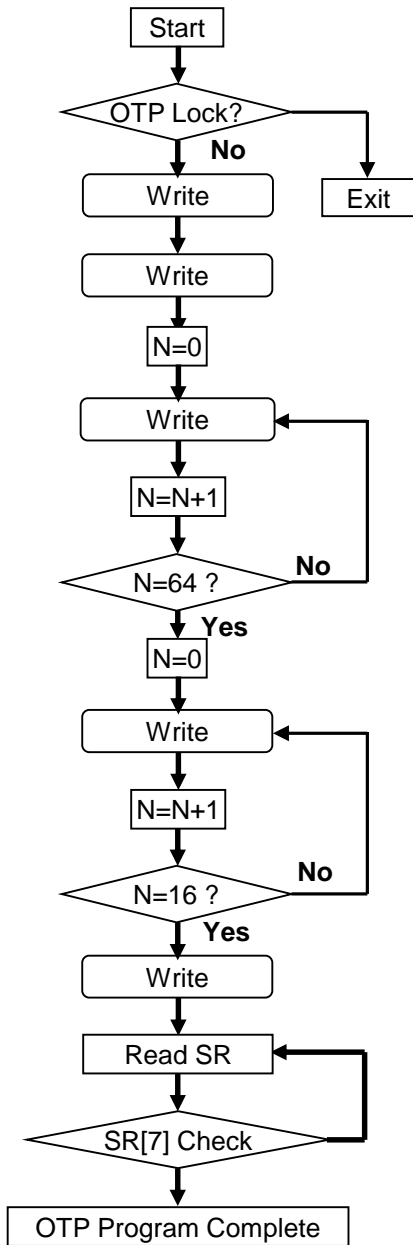
1Gbit NOR type B4-Flash

[64M by 16bit]

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[Program Flow Chart for User OTP Area]



Command	Address	Word Data
---------	---------	-----------

User OTP Setup	OTP ADD	XXC1h
User OTP Page Program Setup	OTP Page ADD	XX4Fh

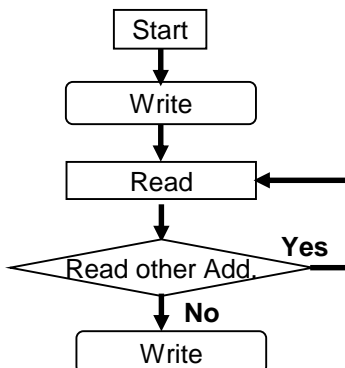
User OTP Page Program Load	OTP Word ADD(0) to OTP Word ADD(63)	PD(0) to PD(63)
----------------------------	--	--------------------

User OTP Page Program Confirm 1	OTP Word ADD(64) to OTP Word ADD(79)	0000h
---------------------------------	---	-------

User OTP Page Program Confirm 2	OTP ADD	XXD0h
---------------------------------	---------	-------

Check SR[7]	Data
WSM Ready	1
WSM Busy	0

[Read Flow Chart of User OTP Area]



Command	Address	Word Data
---------	---------	-----------

User OTP Entry	OTP ADD	XXC1h
----------------	---------	-------

Need 1ms wait time after command input of read of User OTP Area.

Exit User OTP Read	Don't Care	XXFFh
--------------------	------------	-------

G78FVW001KSQAE**1Gbit NOR type B4-Flash**

[64M by 16bit]

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Absolute Maximum Ratings

Symbol	Parameter	Condition	Min.	Max.	unit
VCC	VCC Supply Voltage	Referenced to VSS	-0.2	2.5	V
VCCQ	VCCQ Supply Voltage		-0.2	4.0	V
VI1	Input Voltage		-0.5	VCCQ+0.5	V
Tbs	Storage Temperature w/ Bias		-50	95	°C
Tstg	Storage Temperature w/o Bias		-65	125	°C
Iout	Output Short Circuit Current			100	mA

Operating Ranges

Symbol	Parameter	Min.	Max.	unit
VCC	VCC Supply Voltage	1.7	2.0	V
VCCQ	VCCQ Supply Voltage	2.7	3.6	V
Ta	Ambient Operation Temperature	-40	85	°C

G78FVW001KSQAE**1Gbit NOR type B4-Flash**

[64M by 16bit]

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DC Characteristics(1)

Symbol	Parameter	Condition	Min.	Typ.	Max.	unit
ILI	Input Leakage Current	$0V \leq V_{IN} \leq V_{CCQ}$			± 2	μA
ILO	Output Leakage Current	$0V \leq V_{OUT} \leq V_{CCQ}$			± 2	μA
ICC1	Read Current	Random Read		40	65	mA
		Page Read	$C_{En\#}=V_{IL}, OE\#=V_{IH}, f=20MHz$	12	20	mA
ICCR	Reset Current	$RESET\#=GND$		70	200	μA
ICC2	Standby Current	$CE1\#=CE2\#=RESET\#=V_{CCQ} \pm 0.2V$		740	1000	μA
ICC3	Program Current			35	45	mA
ICC4	Erase Current			32	40	mA
VLKO	VCC Lock Voltage		1.0			V

Caution: $C_{En\#}$ ($n=1,2$) must not be "L", simultaneously. When $C_{En\#}$ ($n=1,2$) is "L", $C_{Em\#}$ ($m < n$) must be remained "H".

DC Characteristics(2) [VCCQ=2.7V-3.6V]

Symbol	Parameter	Condition	Min.	Typ.	Max.	unit
VIL	Input Low Voltage	$V_{CC} \geq 2.7V$	-0.5		0.8	V
VIH	Input High Voltage		$0.7V_{CCQ}$		$V_{CCQ} + 0.4$	V
VOL	Output Low Voltage	$V_{CC}=V_{CCMin}, V_{CCQ}=V_{CCQMin}, I_{OL}=100\mu A, I_{OH}=-100\mu A$			$0.15V_{CCQ}$	V
VOH	Output High Voltage		$0.85V_{CCQ}$			V

Input / Output Capacitance

Symbol	Parameter	Condition	Min.	Max.	unit
CIN	Input Capacitance	$V_{IN}=0V$	TBD	24	pF
COUT	Output Capacitance	$V_{OUT}=0V$	TBD	24	pF

G78FVW001KSQAE

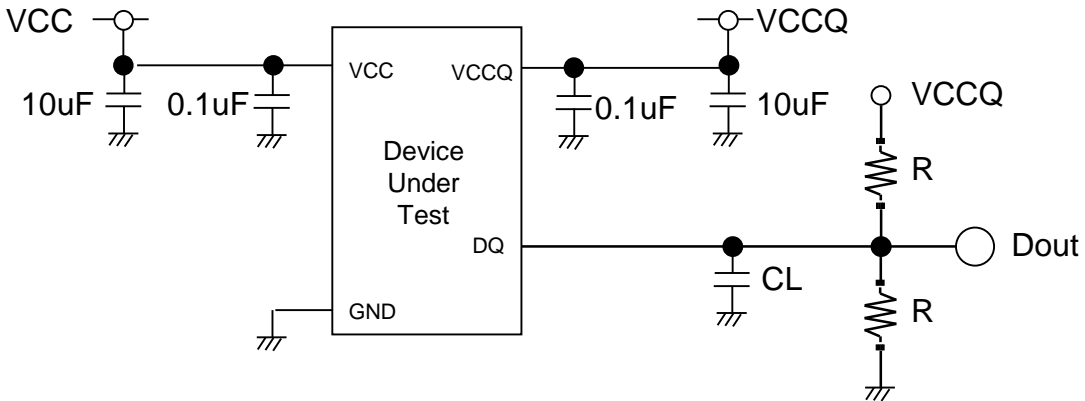
1Gbit NOR type B4-Flash

[64M by 16bit]

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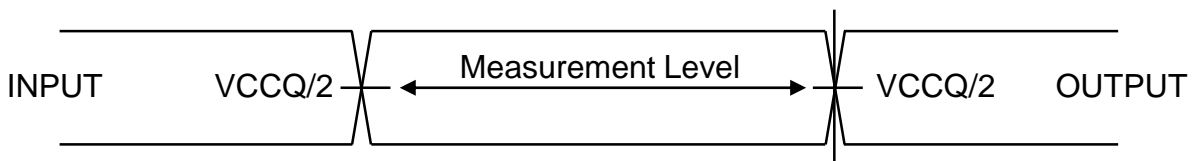
[AC Test Conditions]



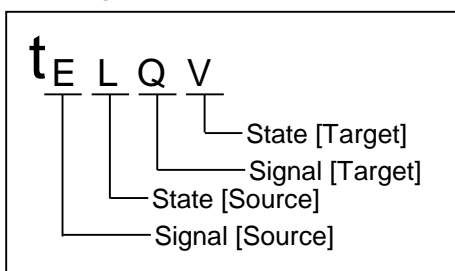
VCC	VCCQ	R(Ohm)
1.8V	3.3V	16.5K

AC Measurement Conditions

Parameter	Min.	Max.	unit
VCC	1.7	2.0	V
VCCQ	2.7	3.6	V
Output Load Capacitance	30		pF
Input Rise and Fall Time		3	ns
Input pulse Level	0	VCCQ	V
Output timing reference level	VCCQ/2		V
Ambient Temperature	-40	85	°C



Timing Symbol Notation



Signal	Symbol	State	Symbol
Address	A	High	H
Data -Read	Q	Low	L
Data - Write	D	High-Z	Z
Chip Enable (CEn#)	E	Low-Z	X
Output Enable (OE#)	G	Valid	V
Write Enable (WE#)	W	Invalid	I
Reset (RESET#)	P		

G78FVW001KSQAE

1Gbit NOR type B4-Flash

[64M by 16bit]

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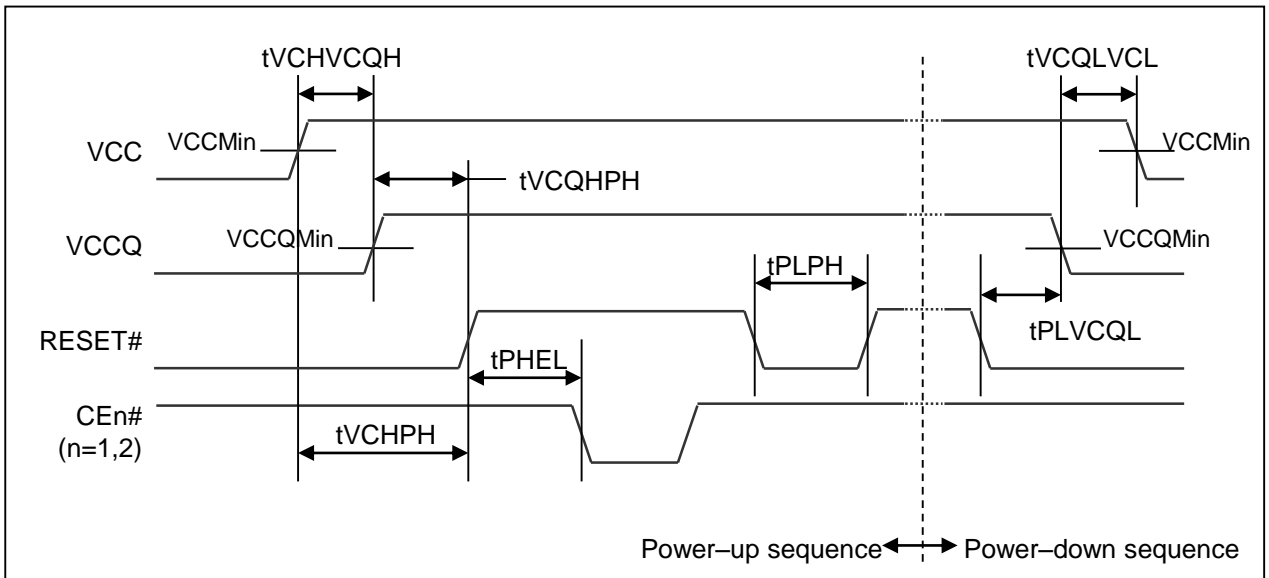
Power up and Reset Timings

Proper Power-up sequence is required to keep the device stable.

- 1) During power up, RESET# must be kept "L". RESET# must stay "L" for more than t_{VCHPH} and t_{VCQHPH} , after VCC reaches to V_{CCmin} and VCCQ to V_{CCQmin} .
- 2) After that, RESET# signal can be set "H".
- 3) After RESET# become "H", CEn# must be kept "H" in the period of t_{PHEL} .

Also, to reset the device effectively, more than the period of t_{PLPH} is required.

Symbol	Parameter	Min.	Max.	unit
$t_{VCHVCQH}$	VCC High to VCCQ High	0		us
$t_{VCQLVCL}$	VCCQ Low to VCC Low	0		us
t_{VCHPH}	VCC High to RESET# High	100		us
t_{VCQHPH}	VCCQ High to RESET# High	0		us
t_{PHEL}	RESET# High to CEn# Low	300		us
t_{PLPH}	RESET# Low to High, RESET# Pulse Width	100		us
t_{PLVCQL}	RESET# Low to VCCQ Low	0		us



Caution: CEn# (n=1,2) must not be "L", simultaneously. When CEn#(n=1,2) is "L", CEm#(m<>n) must be remained "H".

G78FVW001KSQAE**1Gbit NOR type B4-Flash**

[64M by 16bit]

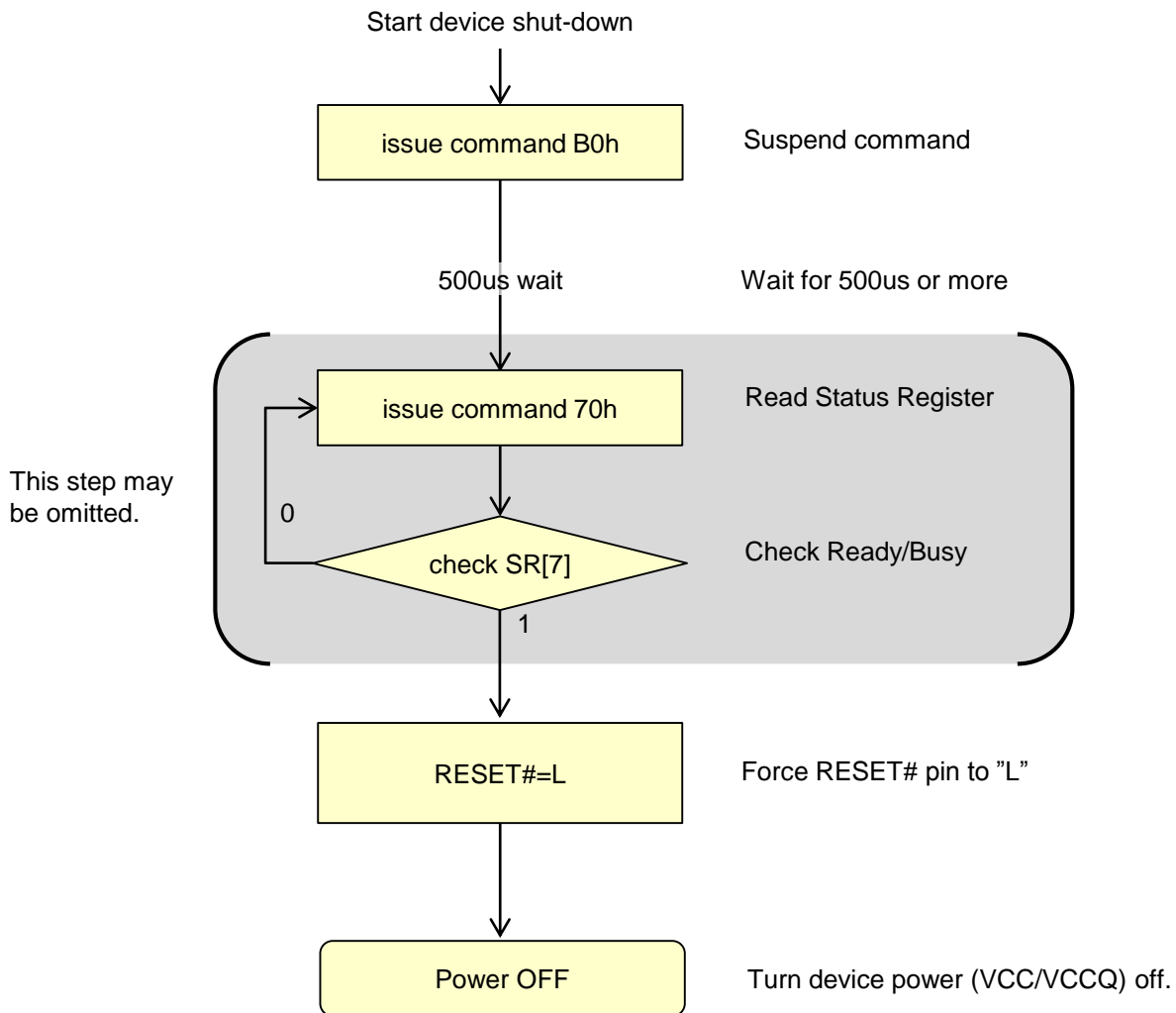
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[Suspend command and shut down sequence]

This device has a suspend command which temporally stops internal operation of program or erase sequence. (please see p.9, p.15, p16)

By using steps below, the command is also usable to avoid interferences during device shutting down.



G78FVW001KSQAE**1Gbit NOR type B4-Flash**

[64M by 16bit]

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AC Characteristics [Page Read]

Symbol	Parameter	Min.	Max.	unit
tAVAV1	Address Valid to Next Address Valid for A0~A3 (1st Access), 1st Access Read Cycle Time (A0~A3) Vcc : 1.7V~2.0V	115		ns
tAVAV1	Address Valid to Next Address Valid for A0~A3 (1st Access), 1st Access Read Cycle Time (A0~A3) Vcc : 1.8V~2.0V	100		ns
tAVAV2	Address Valid to Next Address Valid for A0~A3 (2nd Access), 2nd Access Read Cycle Time (A0~A3)	30		ns
tAVAV	Address Valid to Next Address Valid for A4~Amax, Read Cycle Time (A4~Amax) Vcc : 1.7V~2.0V	180		ns
tAVAV	Address Valid to Next Address Valid for A4~Amax, Read Cycle Time (A4~Amax) Vcc : 1.8V~2.0V	150		ns
tAVQV	Address Valid to Output Valid Vcc : 1.7V~2.0V		115	ns
tAVQV	Address Valid to Output Valid Vcc : 1.8V~2.0V		100	ns
tAVQV1	Address Valid to Output Valid (Page)		30	ns
tELEL	CE# Low to CE# Low Vcc : 1.7V~2.0V	180		ns
tELEL	CE# Low to CE# Low Vcc : 1.8V~2.0V	150		ns
tEHEL	CE# High to CE# Low, CE# Pulse Width High	20		ns
tEHAV	CE# High to Address Valid	5		ns
tELEL	Address Valid to CE# Low, Address Setup Time	0		ns
tELAX	CE# Low to Address Transition Vcc : 1.7V~2.0V	115		ns
tELAX	CE# Low to Address Transition Vcc : 1.8V~2.0V	100		ns

Above AC timing specifications are valid in "Page Read Operation"

G78FVW001KSQAE

1Gbit NOR type B4-Flash

[64M by 16bit]

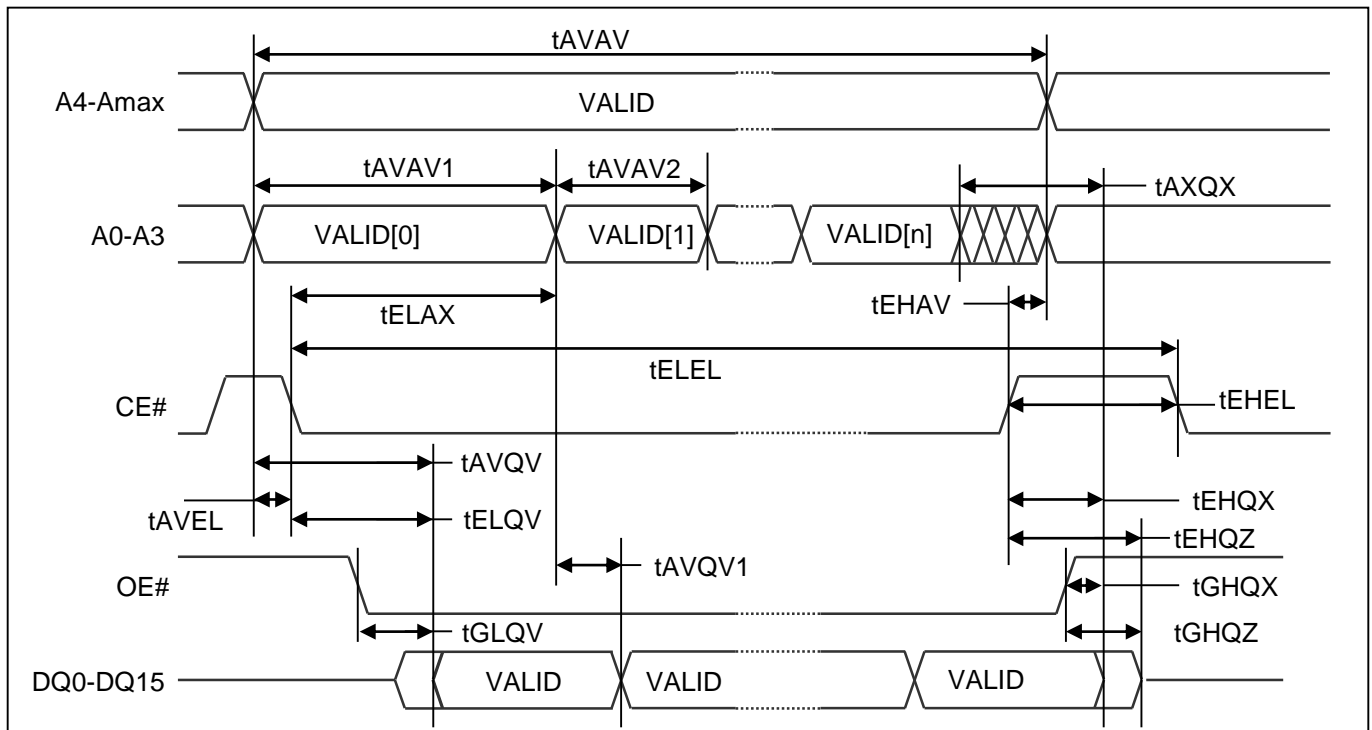
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AC Characteristics [Page Read] (cont'd)

Symbol	Parameter	Min.	Max.	unit
tELQV	CE# Low to Output Valid Vcc : 1.7V~2.0V		115	ns
tELQV	CE# Low to Output Valid Vcc : 1.8V~2.0V		100	ns
tGLQV	OE# Low to Output Valid		30	ns
tEHQZ	CE# High to Output Hi-Z		20	ns
tGHQZ	OE# High to Output Hi-Z		15	ns
tEHQX tGHQX tAXQX	CE#, OE#, Address Transition to Output Transition	0		ns

Above AC timing specifications are valid in "Page Read Operation"



G78FVW001KSQAE

1Gbit NOR type B4-Flash

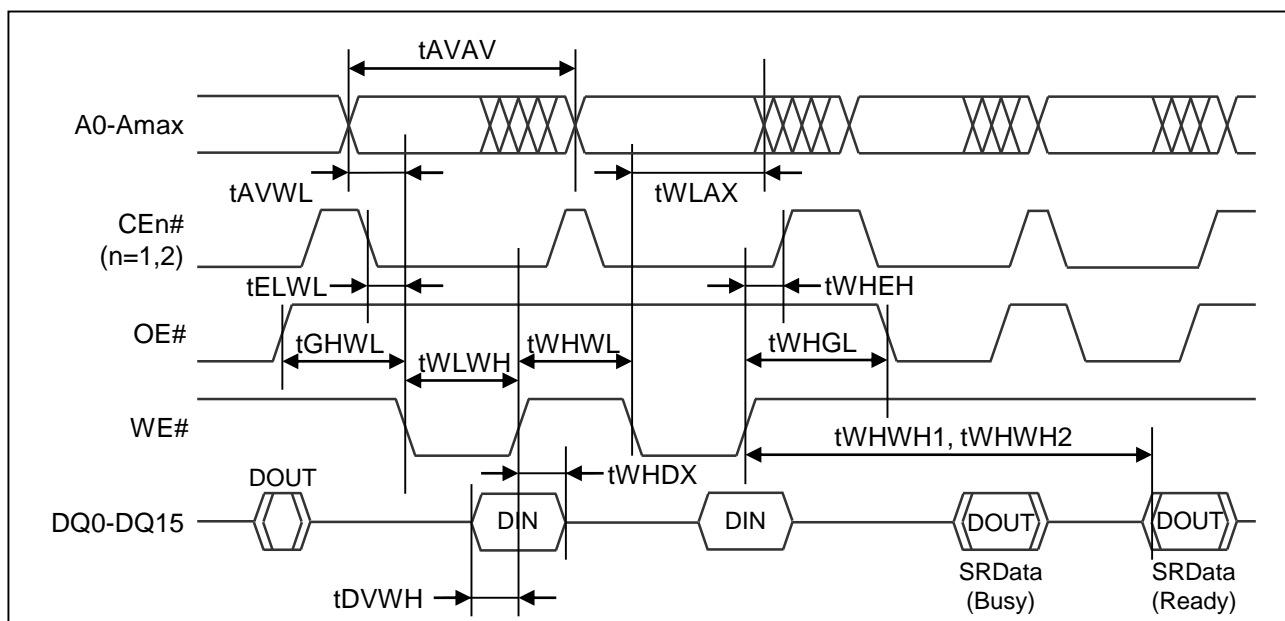
[64M by 16bit]

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AC Characteristics [Write (WE# Controlled)]

Symbol	Parameter	Min.	Max.	unit
tAVAV	Address Valid to Next Address Valid, Write Cycle time	75		ns
tELWL	CEn# Low to WE# Low, CEn# Setup Time	0		ns
tWLWH	WE# Low to WE# High, Write Pulse Width	35		ns
tDVWH	Input Valid to WE# High, Data Setup Time	30		ns
tWHDX	WE# High to Input Transition, Data Hold Time	0		ns
tWHEH	WE# High to CEn# High, CEn# Hold Time	0		ns
tHWWL	WE# High to WE# Low, Write Pulse Width High	30		ns
tAVWL	Address Valid to WE# Low, Address Setup Time	0		ns
tWLAX	WE# Low to Address Transition, Address Hold Time	45		ns
tGHWL	OE# High to WE# Low, OE# Setup Time	0		ns
tWHGL	WE# High to OE# Low, OE# Hold Time	0		ns



Caution: CEn# (n=1,2) must not be "L", simultaneously. When CEn#(n=1,2) is "L", CEm#(m<>n) must be remained "H".

G78FVW001KSQAE

1Gbit NOR type B4-Flash

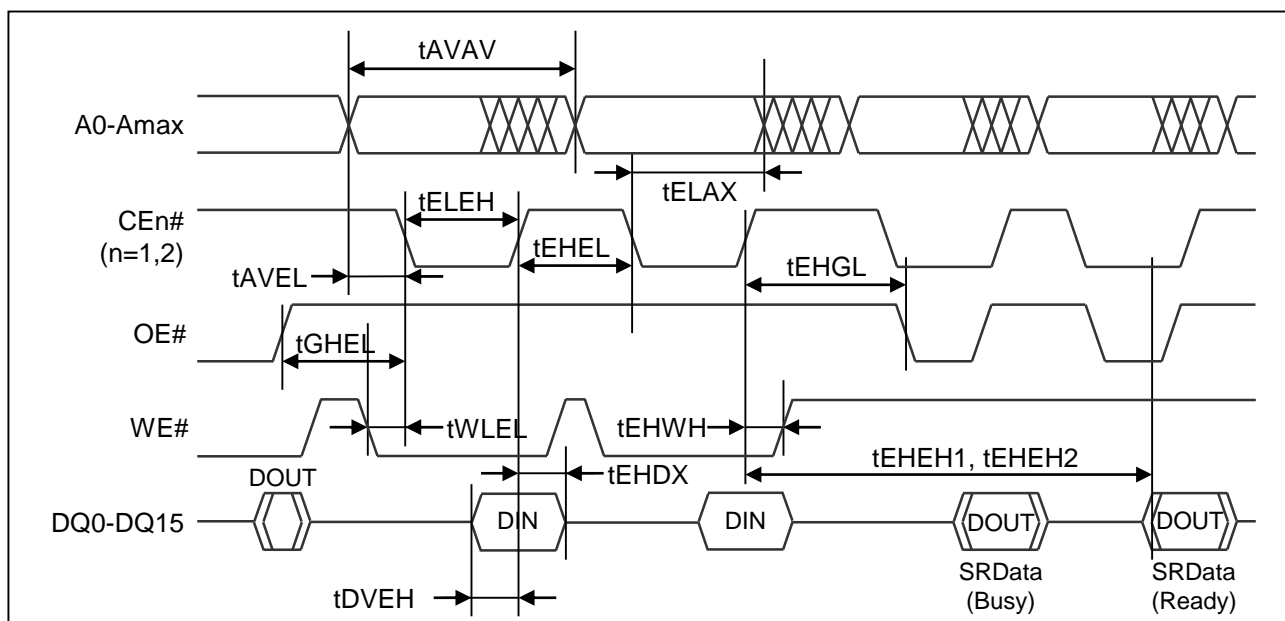
[64M by 16bit]

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AC Characteristics [Write (CEn# Controlled)]

Symbol	Parameter	Min.	Max.	unit
tAVAV	Address Valid to Next Address Valid, Write Cycle time	75		ns
tWLEL	WE# Low to CEn# Low, WE# Setup Time	0		ns
tELEH	CEn# Low to CEn# High, CEn# Pulse Width	35		ns
tDVEH	Input Valid to CEn# High, Data Setup Time	30		ns
tEHDX	CEn# High to Input Transition, Data Hold Time	0		ns
tEHWH	CEn# High to WE# High, WE# Hold Time	0		ns
tEHEL	CEn# High to CEn# Low, CEn# Pulse Width High	30		ns
tAVEL	Address Valid to CEn# Low, Address Setup Time	0		ns
tELAX	CEn# Low to Address Transition, Address Hold Time	45		ns
tGHLE	OEn# High to CEn# Low, OE# Setup Time	0		ns
tEHGL	CEn# High to OE# Low, OE# Hold Time	0		ns



Caution: CEn# (n=1,2) must not be "L", simultaneously. When CEn#(n=1,2) is "L", CEm#(m<n) must be remained "H".

G78FVW001KSQAE**1Gbit NOR type B4-Flash**

[64M by 16bit]

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Program and Erase Characteristics

Operation		Parameter	Min.	Typ.*	Max.*	unit
Block Erase	Single	Block Erase Time		100	500	ms
	4 Bank	Multi-Bank Block Erase Time		100	500	ms
	Chip	Chip Erase Time		2	-	sec
Word Program	Single	Word Program Time		115	575	us
Page Program	Single	Page Program Time		115	575	us
	4 Bank	Multi-Bank Page Program Time		150	750	us
	Chip	Chip Program Time		10	-	sec
Suspend Latency		Program Suspend Time			250	us
		Erase Suspend Time			500	us

* Conditions Typ.: VCC=1.8V, Ta=RT

Max.: VCC=Operating VCC Range, Ta=Operating Temperature Range,
Program/Erase cycle=100Kcycle

Program and Erase Endurance and Data Retention

Operation		Parameter	Min.	Typ.	Max.	unit
Program and Erase Cycles (Compliant with JEDEC std. JESD471 *1)	per Block		100K			cycles
Data Retention (Power-Off Data Retention) (Compliant with JEDEC std. JESD471 *2)						
	after 100Kcyc	Data Retention @Ta [125°C]	20			years

(*1): Compliant with JEDEC std. JESD471, "Min." denotes failure rate of 1% per Block.
Indication of "Typ." corresponds to the failure rate of 50% per Block.

(*2): Compliant with JEDEC std. JESD471, "Min." denotes failure rate of 1% per Chip.
Indication of "Typ." corresponds to the failure rate of 50% per Chip.

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[64M by 16bit]

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[Query Identification String]

(G78FVW001KSQAE)

Offset	Length (Byte)	Query Start Location	Query Data	Values	Description
10h	3	10h	0051h	“Q”	Query Unique ASCII string "QRY"
		11h	0052h	“R”	
		12h	0059h	“Y”	
13h	2	13h	0000h	N/A	Primary Algorithm Command Set and Control Interface ID code 16-bit ID code defining a specific algorithm
		14h	0000h	N/A	
15h	2	15h	0040h	offset P=40h	Address for Primary Algorithm Extended Query Table
		16h	0000h		
17h	2	17h	0000h	N/A	Alternative Algorithm Command Set and Control Interface ID code second specific algorithm supported by the device
		18h	0000h		
19h	2	19h	0000h	N/A	Address for Alternative Algorithm Extended Query Table
		1Ah	0000h		

G78FVW001KSQAE**1Gbit NOR type B4-Flash**

[64M by 16bit]

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[Query System Interface Information]

(G78FVW001KSQAE)

Offset	Length (Byte)	Query Start Location	Query Data	Values	Description
1Bh	1	1Bh	0017h	1.7V	Vcc Logic Supply Minimum Program/Erase or Write voltage. -bits 7-4 : BCD value in volts -bits 3-0 : BCD value in 100 mill volts
1Ch	1	1Ch	0020h	2.0V	Vcc Logic Supply Maximum Program / Erase or Write voltage. -bits 7-4 : BCD value in volts -bits 3-0 : BCD value in 100 mill volts
1Dh	1	1Dh	0000h	N/A	Vpp[Programming] Supply Minimum Program / Erase voltage. -bits 7-4 : HEX value in volts -bits 3-0 : BCD value in 100 mill volts
1Eh	1	1Eh	0000h	N/A	Vpp[Programming] Supply Maximum Program / Erase voltage. -bits 7-4 : HEX value in volts -bits 3-0 : BCD value in 100 mill volts
1Fh	1	1Fh	0005h	32us	Typical timeout per single word program, 2 ⁿ us
20h	1	20h	0008h	128us	Typical timeout for maximum-size multi-byte program, 2 ⁿ us
21h	1	21h	0009h	512ms	Typical timeout per individual block erase, 2 ⁿ ms
22h	1	22h	0010h	64sec	Typical timeout for full chip erase, 2 ⁿ ms
23h	1	23h	0002h	128us	Maximum timeout for word program, 2 ⁿ times typical (offset 1Fh)
24h	1	24h	0002h	1024us	Maximum timeout for multi-byte program, 2 ⁿ times typical (offset 20h)
25h	1	25h	0002h	2048ms	Maximum timeout per individual block erase, 2 ⁿ times typical (offset 21h)
26h	1	26h	0002h	256sec	Maximum timeout for chip erase, 2 ⁿ times typical (offset 22h)

G78FVW001KSQAE**1Gbit NOR type B4-Flash**

[64M by 16bit]

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[Device Geometry Definition]

(G78FVW001KSQAE)

Offset	Length (Byte)	Query Start Location	Query Data	Values	Description
27h	1	27h	001Ah	64MB	Device Size = 2 ⁿ in number of bytes
28h	2	28h	0002h	x8/x16, BYTE#	Flash Device Interface Code description
		29h	0000h		
2Ah	2	2Ah	000Ah	1024 bytes	Maximum number of bytes in multi-byte program = 2 ⁿ
		2Bh	0000h		
2Ch	1	2Ch	0001h	Symmetric	Number of Erase Block Regions within device bits 7-0 : number of Erase Block Regions
2Dh	4	2Dh	003Fh	64Block	Erase Block Region 1 Information -bits 15-0 = y : y+1 = Number of Erase Blocks of identical size -bits 31-16 = z : Erase Block within this region are (z) times 256bytes in size within the Region 1
		2Eh	0000h		
		2Fh	0000h	1Mbyte	
		30h	0010h		
31h	4	31h	0000h	N/A	Reserved for future erase block region 2 information
		32h	0000h		
		33h	0000h		
		34h	0000h		
35h	4	35h	0000h	N/A	Reserved for future erase block region 3 information
		36h	0000h		
		37h	0000h		
		38h	0000h		
39h	4	39h	0000h	N/A	Reserved for future erase block region 4 information
		3Ah	0000h		
		3Bh	0000h		
		3Ch	0000h		

G78FVW001KSQAE**1Gbit NOR type B4-Flash**

[64M by 16bit]

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[Primary Algorithm-Specific Extended Query]

(G78FVW001KSQAE)

Offset	Length (Byte)	Query Start Location	Query Data (x16)	Values	Description
40h	3	40h	0050h	"P"	Query Unique ASCII string "PRI"
		41h	0052h	"R"	
		42h	0049h	"I"	
43h	1	43h	0031h	1	Major Version number, ASCII
44h	1	44h	0030h	0	Minor Version number, ASCII
45h	1	45h	0006h	Not Required / Rev.1.	Address sensitive unlock: -bit0 to 1: 00 = Required, 01 = Not Required -bit2 to 7: Silicon Revision number
46h	1	46h	0002h	Read & Write	Erase Suspend: 00 = not supported, 01 = Read only, 02 = read and write
47h	1	47h	0001h	1	Block Protection: 00 = not supported, x = number of blocks per group
48h	1	48h	0001h	Supported	Temporary block unprotect: 00 = not supported, 01 = supported
49h	1	49h	0000h	Original	Block Protect and Unprotect: 00=Original
4Ah	1	4Ah	0000h	N/A	Simultaneous operation
4Bh	1	4Bh	0000h	N/A	Burst mode: 00 = not supported, 01 = supported
4Ch	1	4Ch	0003h	16word	Page mode Read : 00 = Not supported 01 = 8word , 02 = 8word , 03 = 16word
4Dh	1	4Dh	0000h	N/A	Vpp Supply maximum Program/Erase voltage bit7 to 4: HEX value in volts bit3 to 0: BCD value in 100m volts
4Eh	1	4Eh	0000h	N/A	Vpp Supply Optimum Program/Erase voltage bit7 to 4: HEX value in volts bit3 to 0: BCD value in 100m volts
4Fh	1	4Fh	0000h	N/A	Top / Bottom boot block flag 04h = Symmetrically block and H/W protect for lowest block 05h = Symmetrically block and H/W protect for highest block
50h	1	50h	0001h	Supported	Program Suspend: 00 = not supported, 01 = supported

G78FVW001KSQAE

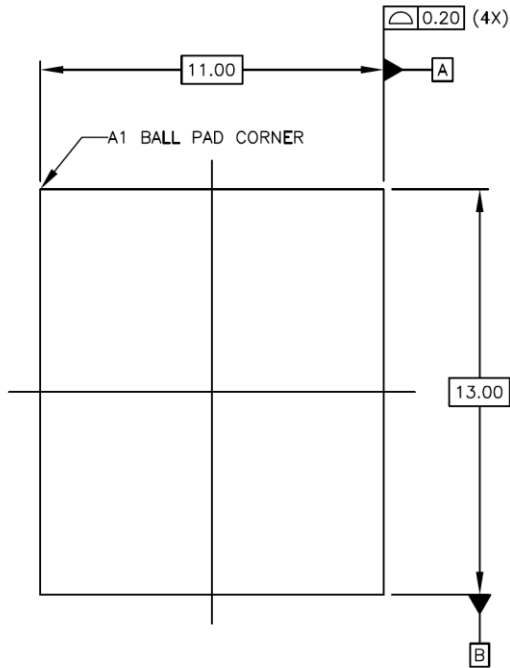
1Gbit NOR type B4-Flash

[64M by 16bit]

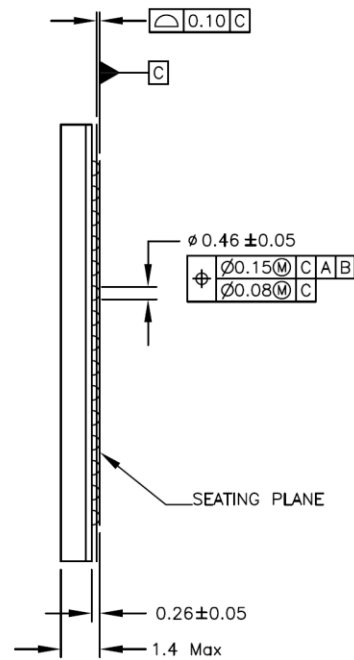
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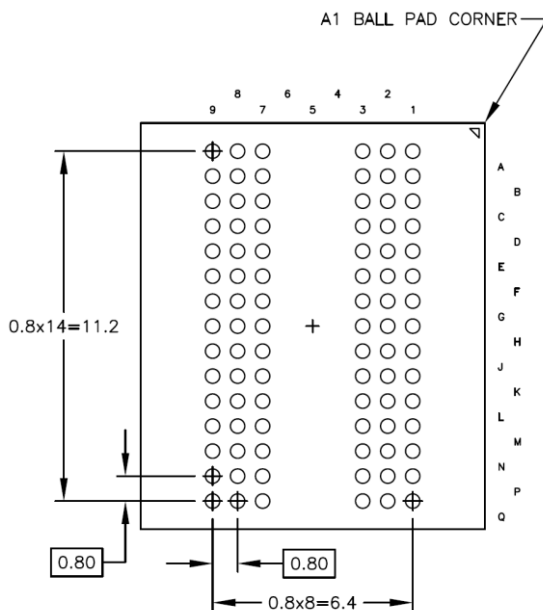
G78FVW001KSQAE Package Outline



TOP VIEW



SIDE VIEW



BOTTOM VIEW
90 SOLDER BALLS